2-nm-EOT Y-Si-O Gate Stack Formation on $Si_{0.5}Ge_{0.5}$

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Introduction

SiGe with a small percentage of Ge is carefully characterised [1] and practically used, while Ge rich SiGe (% of Ge ≥ 50%) still possesses a big challenge due to a lack of device quality gate stack formation. This work reports a well-controlled $Si_{0.5}Ge_{0.5}$ interface with thin Y-Si-O film.

Results and Discussion

It is known that GeO_2 on Ge is intrinsically unstable, resulting in GeO desorption and degradation of Ge gate stack [2]. We conjectured that this should also be an issue for Ge-rich SiGe case. Therefore, we put two requirements as folllows. (i) Ge oxidation should be as slight as possible. (ii) The dielectric film should be as energetically stable as possible. In order to satisfy two challenges, we employed YSiO for the dielectric film and O_2-PDA, because Y_2O_3 is the most stable oxide in terms of the Gibbs free energy but with a large oxygen diffusion constant.

The starting substrate was 110 nm $Si_{0.5}Ge_{0.5}$(100) on p-Si(100) with resistivity of 5-100 Ω–cm. 5-nm-thick YSO was deposited directly on the substrate by RF co-sputtering of Y_2O_3 and SiO_2, followed by O_2-PDA, in which Y:Si ratio and O_2 ocncentration were changed to find the best spot. First, no Ge oxidation of SiGe was observed by XPS even at 600°C in O_2 for 30 sec, as shown in **Fig. 1**. **Fig. 2** shows C-V characteristics of SiGe gate stack with the same PDA as that of Fig. 1. The result looks remakably good, including frequency dispersion. In case of (O_2+N_2) ambient, C-V characteristics were obviously degraded (data not shown). Effects of the forming gas annealing (FGA) were also investigated at 400, 450 and 500°C. None of these conditions can effectively improve the interface properties. Furthermore, effect of Y:Si ratio in YSO was studied from 20% to 70%, and 50% was the best so far, which is shown in Fig. 2. Finally, the surface morphology of SiGe by removing YSO. The so-called crosshatch patterns can be clearly seen on SiGe surface after PDA at 600°C (**Fig. 3**). This fact suggests that electrical properties are not degarded by those patters in the present case. Finally, it should be mentioned that the present results are quite consistent with the robust YGO (Y-doped GeO_2) film [3].

Conclusions

We have demonstrated well-controlled SiGe gate stacks using YSO. Key points in this study are three-fold: no Ge oxidation, sufficient oxygen suppy into gate stacks and slow oxgyen diffusion in dielectrics.

Reference

[1] J. Han et al., APEX 6 (2013) 051302.[2] S. K. Wang et al., J. Appl. Phys. **108**, 054104 (2010).[3] C. Lu, et al., J. Appl. Phys. **116**, 174103 (2014).

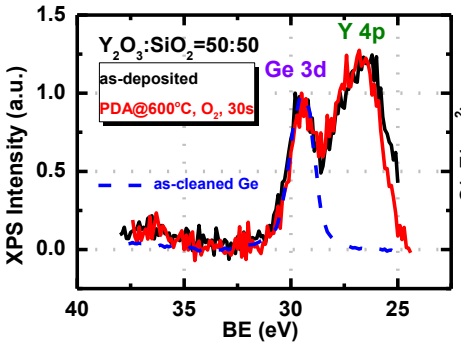

Fig. 1 Ge and Y XPS spectrum of $YSO/Si_{0.5}Ge_{0.5}$ before and after PDA. Compared with the as-cleaned Ge substrate, no Ge oxidation is observed after PDA@600°C, O_2, 30 sec.

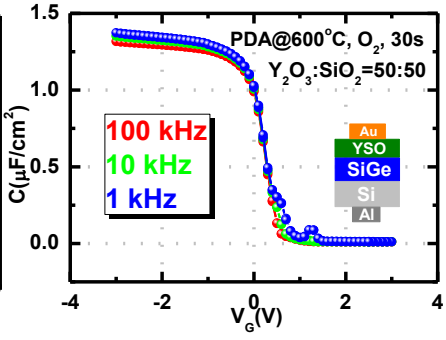

Fig. 2 CV of $YSO/Si_{0.5}Ge_{0.5}$ (Y = 50%) with PDA@600°C, O_2, 30s. The area of the Au electrode is 10^{-4} cm^{-2}.

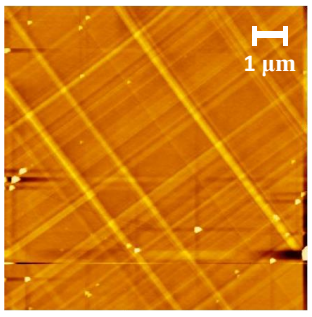

Fig. 3 AFM of the interface of $YSO/Si_{0.5}Ge_{0.5}$ (Y = 50%) with PDA@600°C, O_2, 30s after YSO removal by HCl and HF. The size of the image is 10 μm by 10 μm.