# Patterning of High-k/metal gate Stack by Neutral Beam Etching Technique for Sub-20 nm CMOS Technology

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As the minimum feature size of microelectronic devices shrinks down to 20 nm and beyond, the conventional poly-Si gate is encountering severe problems such as the poly depletion effect and the increase in leakage current, which is currently replaced by high-k/metal gate stack to keep the electrical performance of CMOSFETs. However, as the high-k material is adopted in the gate electrode, damages by plasma charging effect which could be tolerated in thin $SiO_2$ is now reintroduce on the scene[1]. As a result, in this study we used a neutral beam etching (NBE) technique to pattern high-k/metal gate stack as an alternative for conventional inductively-coupled plasma (ICP) etching. The NBE technique is anticipated to eliminate dielectric damage caused by the charge buildup, and also defects generated by the radiation of UV and X-ray photons[2].

In this work, a PVD TiN/ALD TiN/ALD $HfO_2$/Si gate stack, as shown in figure 1, is prepared and etched by NBE with Ar and $Cl_2$ gas mixture. Etching properties on thin films of TiN, $HfO_2$ and $SiO_2$ was studied with respect to Ar and $Cl_2$ gas mixing ratio and bias power. Figure 2 shows that the highest etch rate of 2 nm/min for $HfO_2$ and 6 nm/min for TiN can be achieved when using an Ar/(Ar+$Cl_2$)=60% mixture, and no under-cut was observed on all the samples. Furthermore, the etching results of TiN thin films was found to be highly dependent on the structure and preferred orientation, and the roughness can be reduced by modifying film structure and bias power. In conclusion, the TiN/$HfO_2$/Si gate stack was successfully etched by NBE technique with an Ar and $Cl_2$ gas mixture. Further experimental details and results will be presented in the conference.

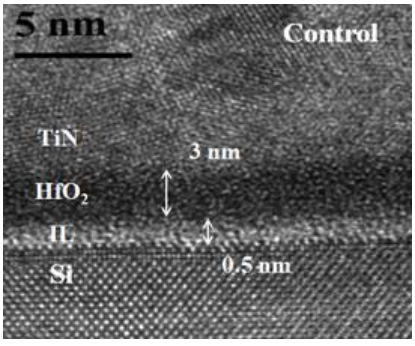


Fig. 1 TEM image of TiN/$HfO_2$ gate stack

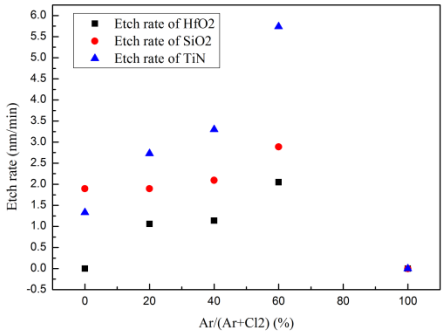


Fig. 2 Etch rate as functions of Ar+$Cl_2$ mixing ratio

**References:**

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