In-situ Formation of HfN_x Gate Stack Structures Utilizing ECR Plasma Sputtering

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1. Introduction

Scaling down an equivalent oxide thickness (EOT) of metal/high-κ gate stack beyond 0.5 nm is a great challenge for next generation CMOS technology because of the formation of low-κ interfacial layer (IL) between high-κ/Si interfaces [1]. We have reported that 0.5 nm EOTs were obtained by using hafnium nitride (HfN) gate insulator formed by electron-cyclotron-resonance (ECR) plasma sputtering with Al electrode [2].

In this paper, *in-situ* formation of high thermal stability metallic-phase HfN_x, ($x < 1$) on HfN gate insulator for gate-first process [3] was investigated utilizing ECR plasma sputtering.

2. Experimental Procedure

First, p-Si(100) substrates were cleaned by SPM and DHF. Then HfN gate insulator (4.9 nm) was deposited by ECR plasma sputtering with the gas pressure of 0.20 Pa (Ar/N_2: 20/8 sccm) [4]. The metallic-phase HfN_x electrode (70 nm) was *in-situ* deposited with the gas pressure of 0.17 Pa (Ar/N_2: 20/0.4 sccm). After gate electrode patterning by lithography, HfN gate stack was patterned by DHF (1%) for 140 s. Finally, backside Al contact was deposited by evaporation. The sample with Al electrode (ϕ = 94 μm) deposited by evaporation through a shadow mask was fabricated for comparison [5]. The C-V and J-V characteristics of HfN/p-Si(100) MIS-diodes were measured. The x-ray photoelectron spectroscopy (XPS) was carried out to evaluate the depth profile of HfN gate stack.

3. Results and Discussion

Figure 1 shows the depth profile of HfN gate stack. The metallic-phase HfN_x electrode and HfN gate insulator has N/Hf atomic ratio of 0.68:1 and 1:1, respectively. The oxygen content at the HfN/Si interface is below 3.6%. This means, *in-situ* deposition of HfN gate stack can suppress the oxygen incorporation and the formation of IL. The results in Fig. 2 show the C-V characteristics (100 kHz) of as-deposited HfN MIS-diode with Al and HfN electrode. The EOT (100 kHz) of 0.8 and 0.7 nm with ΔV_{FB} of -0.34 and 0.14 V were obtained by using HfN (ϕ_{HfN}: 4.8 eV) and Al electrode (ϕ_{Al}: 4.1 eV), respectively. The V_{FB} shifted towards negative direction might due to the plasma damage during deposited HfN electrode. The suppression of leakage current density, (J_g @V_{FB} -0.5 V), of HfN electrode (6.0×10^{-5} A/cm^2) compared to Al electrode (1.3 A/cm^2) might due to the *in-situ* process that leads to the excellent interface properties and film qualities.

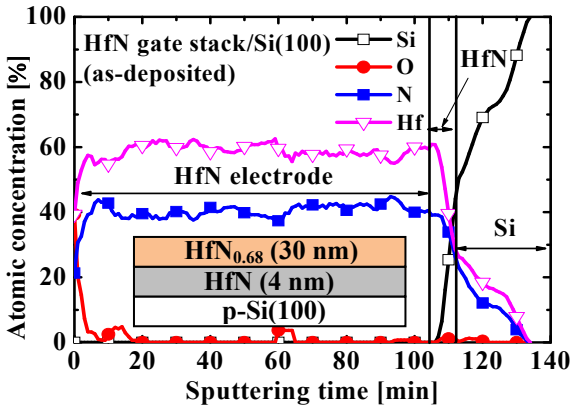

Fig. 1. Depth profile of *in-situ* HfN gate stack structure formed by ECR plasma sputtering.

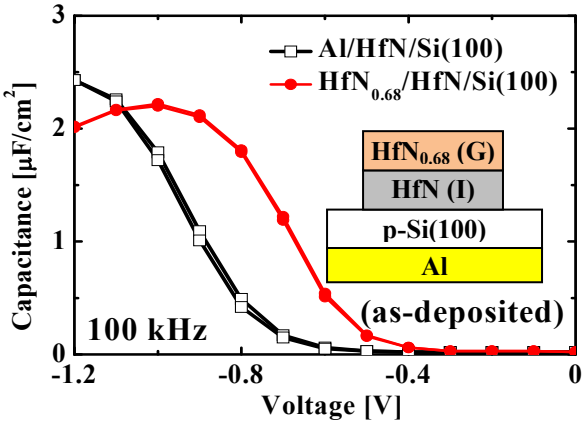

Fig. 2. C-V characteristics (100 kHz) of as-deposited HfN/p-Si(100) MIS-diode with Al and HfN gate electrode.

4. Conclusions

We investigated the *in-situ* formation of HfN gate stack utilizing ECR plasma sputtering. The *in-situ* deposition of HfN electrode can suppress the oxygen incorporation and IL formation, which can improve the electrical properties of HfN MIS-diode.

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