## Electrostatic Carrier Doping to KTaO<sub>3</sub> Using Organic Parylene-C/High-*k* Oxide Hybrid Gate Insulator

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Electric-field control of electronic properties of functional oxides using field-effect transistor structures (FETs) has been attracting attention [1]. However, the overlayer deposition of gate insulator onto oxide channel often involves irreversible damages on the channel surface such as redox reactions, making it difficult to observe intrinsic carrier doping effects. Recently, Eyvazov *et al.* proposed that the insertion of organic polymer parylene-C between the gate oxide dielectric and

the SrTiO<sub>3</sub> channel is effective for suppressing those damages on the channel surface [2]. In this work, we attempted carrier injection into KTaO<sub>3</sub> band insulator using a hybrid gate insulator consisted of organic polymer parylene-C and high-k oxide Ta<sub>2</sub>O<sub>5</sub>.

A FET structure was fabricated utilizing a single-crystalline KTaO<sub>3</sub>(001) substrate as the channel (Fig. 1). Al electrodes (20 nm-thick), parylene-C (70 nm-thick), and Y-doped Ta<sub>2</sub>O<sub>5</sub> film (210 nm-thick) were synthesized by e-beam deposition, chemical vapor deposition, and rf sputtering, respectively. KTaO<sub>3</sub> FETs with Y-doped Ta<sub>2</sub>O<sub>5</sub>/parylene-C gate structure showed typical *n*-type behavior with clear saturation characteristics, as displayed in Fig. 2. The on/off ratio and field-effect mobility reached  $10^4$  and  $0.1 \text{ cm}^2/\text{Vs}$ , respectively, which were much higher than KTaO<sub>3</sub> devices with bare Y-doped Ta<sub>2</sub>O<sub>5</sub> insulator. This suggests that the insertion of parylene-C, which possesses high chemical stability and mild deposition conditions, prevents the degradation of the KTaO<sub>3</sub> surface during the gate insulator fabrication process effectively. Effect of the thicknesses of the two dielectric layers on FETs characteristics will also be presented.

[1] C. H. Ahn et al., Rev. Mod. Phys. 78, 1185 (2006).

[2] A. B. Eyvazov et al., Sci. Rep. 3, 1721 (2013).

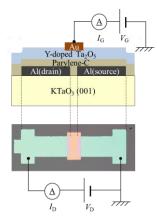


Fig. 1. Schematic structure and top-view photograph of a KTaO<sub>3</sub>-FET. Channel length *L* and width *W* were 200  $\mu$ m and 400  $\mu$ m, respectively.

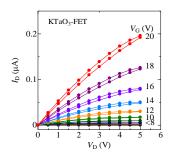


Fig. 2. Output characteristics of a KTaO<sub>3</sub>-FET at room temperature.