Design of High-k and Interfacial Layer on Germanium for 0.5 nm EOT

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[Introduction] Prominent interface passivation of Ge has been demonstrated by several GeO₂-based dielectrics as interfacial layer (IL) between Ge and high-k [1-4]. However, with the progressive EOT scaling, reduction of IL thickness to a few angstroms is expected, where the interface properties become highly sensitive to the high-k dielectrics as well. Thus, high-k should be designed consistently with GeO₂-based IL with respect to both interface property and EOT scalability. This work is to provide a guiding principle on high-k dielectric design for Ge gate stack formation in 0.5 nm EOT region.

[Experiment] Various thicknesses of yttrium doped GeO₂ (Y-GeO₂) was deposited on HF-last pGe substrate as IL by rf co-sputtering of GeO₂ and Y₂O₃ targets. After the deposition of Y-GeO₂ IL, YScO₃ was also deposited by co-sputtering as high-k dielectrics. Post deposition annealing (PDA) was carried out at 500°C in N₂/O₂ (0.1%) ambient for 30 second. For comparison, HfO₂/Y-GeO₂/Ge stacks were prepared in the same manner. To characterize the electrical properties, Au and Al were deposited by vacuum evaporation for the gate electrode and substrate contact of the MOSCAPs, respectively.

[Results and discussion] Regardless of the promising interface passivation offered by Y-GeO₂ IL [4], the electrical properties of the entire gate stack are strongly influenced by top high-k due to its intermixing with GeO₂-based IL. Thus, the selection of cation species for high-k should also take account of their bond configuration at Ge interface as schematically shown in **Fig. (1)**. Cation species like Hf form M-Ge metallic bond at the interface while the counterparts, like Y, are immune to M-Ge bond formation, which is understandable from their different gibbs free energy for germanidation as following equations [5]:

$$\begin{aligned} HfO_2+3Ge=HfGe_2+GeO_2 & \Delta G=-27kcal/mol & (1) \\ Y_2O_3+3.5Ge=2YGe+1.5GeO_2 & \Delta G=152.8kcal/mol & (2) \end{aligned}$$

Since M-Ge bond results in gap state in Ge [5, 6], a proper high-k should consist of cations without M-Ge formation. YScO₃ demonstrates a high-k value of 17 with both Y and Sc immune to metallic bond. A comparison is carried out between YScO₃ and HfO₂ as high-k dielectrics for Ge gate stack. **Fig. 2(a)** shows the D_{it} near the mid-gap as a function of EOT in YScO₃/Y-GeO₂/Ge and HfO₂/Y-GeO₂/Ge stacks measured by high-low-frequency capacitance method. Note that the thicknesses of both high-ks are fixed at 2 nm while the EOT is changed by the Y-GeO₂ IL thickness. It is found that the D_{it} in HfO₂/Y-GeO₂/Ge stacks increases drastically with thinner IL below 1 nm, which indicates that a certain thickness of IL is needed as barrier to block the destructive influence on the interface from HfO₂. On contrary, YScO₃/Y-GeO₂/Ge stacks keep low D_{it} regardless of the IL thickness. Thanks to the interface friendly character of YScO₃, aggressive EOT scaling is obtainable. **Fig. 2(b)** shows the bidirectional *C-V* characteristics of YScO₃/Y-GeO₂/Ge with Y-GeO₂ IL as thin as 0.5 nm. Deep sub-nm EOT and proper interface passivation can be achieved simultaneously in our gate stacks. An affordable gate leakage current about 0.5A/cm² @V_{FB}-1V is also observed in this gate stack. Thus we can conclude that YScO₃ is a promising high-k dielectric for Ge gate stack formation.

[Conclusion] A guideline for high-k design on Ge is proposed that cation species immune to M-Ge metallic bond formation are required. Based on this understanding, 0.5 nm EOT with good interface was demonstrated.

[Reference] [1] C. H. Lee *et al*, *IEEE TED*. **58**, 1295 (2011). [2] S. Takagi *et al.*, *IEDM*, 372 (2012). [3] D. Kuzum *et al.*, *IEEE ED* **58**, 59 (2011). [4] C. H. Lee *et al.*, *IEDM*, 40 (2013). [5] C. Lu *et al.*, *JAP*, **116**, 174103 (2014). [6] M. Houssa *et al.*, *Surface Science*, **602**, L25 (2008).



M-Ge M-Ge

Fig. 1 Schematic of cation selection criterion on cation species for high-k on Ge. M-Ge bond formation should be prevented from the energy viewpoint.

(a) (b) **Fig. 2(a)** $D_{it} @E_i - 0.2 eV$ as a function of EOT in YScO₃/Y-GeO₂/Ge and HfO₂/Y-GeO₂/Ge stacks. (b) Bidirectional *C-V* curves of a (2 nm)YScO₃/(0.5 nm)Y-GeO₂/Ge stack measured at RT.

EOT=0.5 nm

-1

0

Gate voltage (V)

-1MHz

- 10kHz