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Investigation of Bilayer HfN Gate Insulator Formed by ECR Plasma Sputtering

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1. Introduction

We have reported that the equivalent oxide thickness (EOT) of metal/high-κ gate stacks of 0.58 nm was obtained by *in-situ* formation of bilayer hafnium nitride (HfN_x) gate insulator (I) and gate electrode (G) utilizing electron-cyclotron-resonance (ECR) plasma sputtering [1]. However, large hysteresis width (ΔV) of 184 mV and significant flat-band voltage (V_{FB}) shift in C-V characteristics after post-metallization annealing (PMA) in N_2/4.9%H_2 forming-gas (FG) ambient at 500°C/10 min degraded the mobility of nMISFETs [2].

In this paper, the effect of PMA on the performance of nMISFETs with bilayer HfN_x gate insulator utilizing ECR plasma sputtering was investigated.

2. Experimental Procedure

The nMISFETs were fabricated on p-Si(100) substrate (N_A: $1x10^{15}$ cm^{-3}) using gate-last process [1]. After local oxidation of Si (LOCOS) and channel stop ion implantation, source/drain (S/D) regions were formed by implanting PH_3 at 20 keV with a dose of $5x10^{15}$ cm^{-2}. The activation annealing was carried out in N_2 ambient at 1000°C/2 min.

Then, 0.9 nm-thick $HfN_{1.1}$ (IL) (Ar/N_2: 16/12 sccm; 0.20 Pa) was deposited utilizing ECR plasma sputtering followed by *in-situ* deposition of 1.7 nm-thick $HfN_{1.3}$ gate insulator (I) (Ar/N_2: 8/20 sccm, 0.20 Pa). Next, 10 nm-thick $HfN_{0.5}$ gate electrode (G) was *in-situ* deposited on $HfN_{1.3}$ (I) (Ar/N_2: 10/0.2 sccm, 0.09 Pa). The PMA1 process (before Al deposition) was performed by silicon-wafer-covering (SWC) annealing in N_2/4.9%H_2 ambient (1 SLM) at 500°C/1-10 min [2-3]. Then, Al contact layer (40 nm) was *ex-situ* evaporated on $HfN_{0.5}$ (G). After contact holes formation, Al pads were patterned for source, drain and gate electrodes. Some PMA1 sample was annealed in the PMA2 process (after Al contact patterning) using N_2/4.9%H_2 ambient at 300°C/30 min [3]. The channel length (L) was 10 μm and channel width (W) was 90 μm. The I_D-V_D and I_D-V_G of nMISFETs were characterized.

3. Results and Discussion

The C-V characteristics of MIS-diode were shown in Fig. 1(a). By the combination of PMA1 at 500°C/1 min with PMA2 at 300°C/30 min, the EOT of 0.55 nm, V_{FB} of -0.52 V, J_g(@V_{FB} -1V) of $6.6x10^{-5}$ A/cm^2, and D_{it} of $5.6x10^{10}$ $cm^{-2}eV^{-1}$ were obtained. The I_D-V_D characteristics in Fig. 1(b) shows that the drain current drivability has increased from 7.0 to 7.8 μA/μm and extracted saturation mobility (μ_{sat}) has increased from 47 to 81 $cm^2/(Vs)$ compared to the device fabricated with PMA1 at 500°C/10 min. The improvement of the electrical characteristics probably

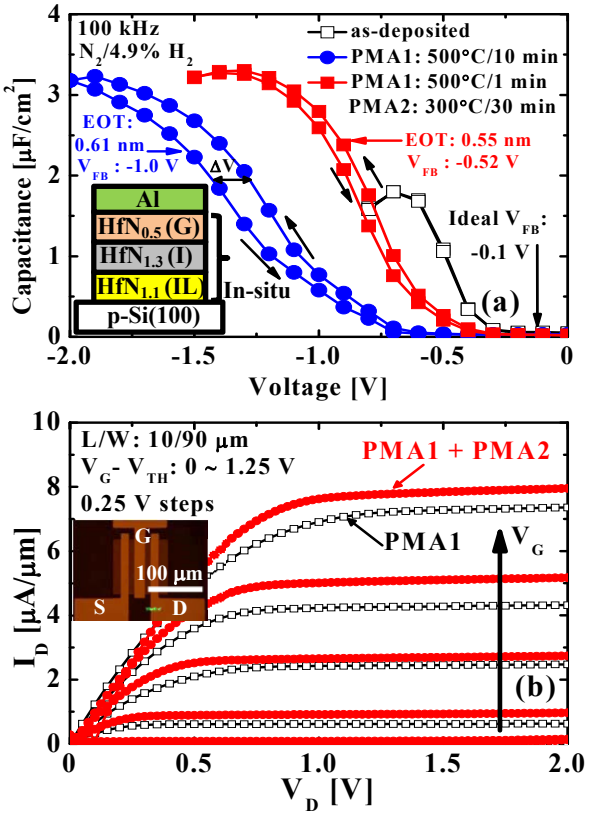

Fig. 1. Effects of post-metallization annealing process on the electrical characteristics of bilayer HfN_x gate insulator. (a) C-V characteristics (100 kHz) of MIS-diode and (b) I_D-V_D characteristics of nMISFETs (L/W: 10/90 μm).

due to PMA2 sintering process such as the decrease hysteresis width from 184 to 54 mV and V_{FB} shift in Fig. 1(a).

4. Conclusions

We investigated the effects of PMA process on the performance of nMISFET with bilayer HfN_x gate insulator utilizing ECR plasma sputtering. The combination of PMA1 and PMA2 processes in N_2/4.9%H_2 ambient showed the suppression of hysteresis width in C-V, which leads to the improvement of the nMISFET characteristics.

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References

[1] N. Atthi and S. Ohmi, The 63rd JSAP spring meeting, 19a-S224-5, p. 11-019 (2016).
[2] N. Atthi and S. Ohmi, IEICE Electron. Exp., **13**, no. 10, pp. 1-6 (2016).
[3] N. Atthi and S. Ohmi, AWAD, B4-3 (2016).