III-V CMOS フォトニクス・プラットフォーム上 キャリア注入型 InGaAsP 可変光減衰器

InGaAsP variable optical attenuator on III-V CMOS photonics platform

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InP-based photonic integrated circuits (PICs) have developed significantly, allowing us to integrate active and passive photonic components monolithically on an InP wafer [1]. However, the weak optical confinement in the conventional InP PICs due to the low refractive index contrast has prohibited us from realizing ultra-small InP PICs in contrast to Si photonics. To overcome this problem, we have proposed the III-V CMOS photonics platform on a III-V on insulator (III-VOI) wafer [2]. To achieve the optical modulation on the III-V CMOS photonics platform, we have explored carrier injection via a lateral PIN junction formed along an InGaAsP waveguide on the III-V-OI wafer. However, the low dopant activation in implanted III-V layers make it difficult to form a low-resistivity lateral PIN junction on the III-V-OI wafer. In this paper, we have introduced the Zn diffusion and Ni-InGaAsP alloying to form a low-resistivity lateral PIN junction [3]. By using this fabrication procedure, we have successfully demonstrated a carrier-injection InGaAsP variable optical attenuator (VOA).

We have performed Zn diffusion from Zn-doped spin-on-glass (SOG) after the waveguide formation at 500 °C. Then, we have formed Ni-InGaAsP alloy instead of n^+-InGaAsP. The Fermi level pinning results in ohmic contact between the Ni-InGaAsP alloy and i-InGaAsP layer. The alloying is carried out by annealing Ni on the InGaAsP layer at 350 °C for 1 min. By using these methods, we have achieved almost 10 and 100 times lower sheet and contact resistances as compared with ion implantation of Si and Be, respectively.

The low-resistivity lateral PIN junction allows us to inject large current into the device, suitable for VOA operation. Fig. 1(a) shows a schematic of carrier-injection InGaAsP VOA on the III-VOI wafer. An InGaAsP rib waveguide on the III-VOI wafer is formed by electron-beam lithography and reactive ion etching. The width of fabricated waveguide is 700 nm. After forming the lateral PIN junction, an SiO_2 passivation layer is deposited by PECVD. Finally, Ti/Pt electrodes are formed by lift-off process. Fig. 2 shows the attenuation characteristic through carrier injection. We have achieved -45dB/mm attenuation at 40 mA/mm current injection, which is approximately 1.7 times greater than that of Si VOAs. Thus, we have successfully demonstrated high-efficient InGaAsP VOA by using Zn diffusion and Ni-InGaAsP alloy on III-V CMOS photonics platform.

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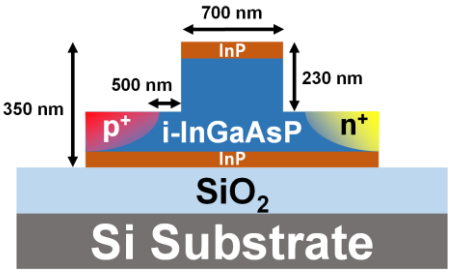

Fig. 1 Schematic of InGaAsP VOA.

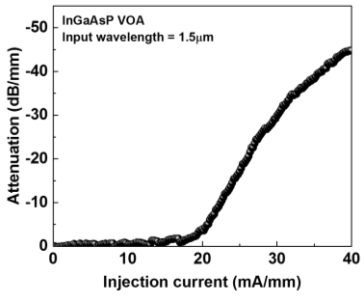

Fig. 2 Attenuation characteristic.