A New Computing Architecture Using Ising Spin Model for Solving Combinatorial Optimization Problems Implemented on FPGA

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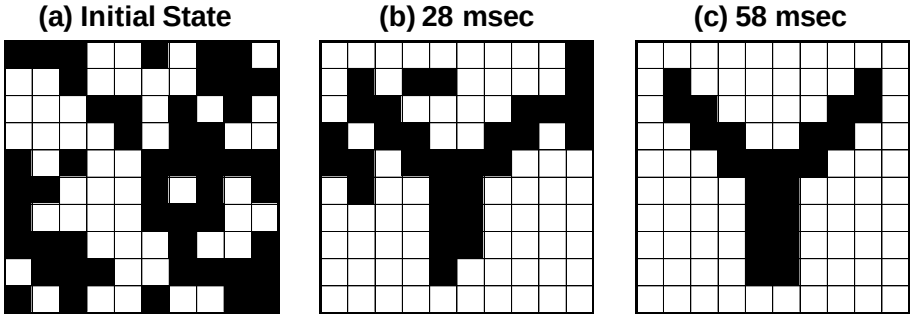
It is well known that Ising spin model represents the physical properties of ferromagnetic materials in terms of statistical mechanics [1]. In this model, the spin states are varied in order to minimize the system energy automatically, by the interaction between connected adjacent spins. The system Hamiltonian H, the total energy of the system, is described using the following formula: $H = -\sum J_{ij}\sigma_i\sigma_j - \sum h_i\sigma_i$, where σ_i and σ_j represent spin states (+1 or –1) at neighboring site i and j, J_{ij} is the interaction coefficient between spins, and h_i is the external magnetic field coefficient. Recently, the new computing architecture called Ising computing has been proposed using superconductors [2] and CMOS circuits [3], to simulate the Ising spin model, in which this method maps the combinatorial optimization problems to the ground state search of the model. In this report, a new computing architecture using Ising spin model was implemented using logic gates, and the Ising computing based on logic gates was investigated to solve combinatorial optimization problems.

First, Ising computing was implemented on a field-programmable gate array (FPGA) and was applied for solving combinatorial optimization problems. Max cut problem was selected as one of the combinatorial optimization problems, where the spin states would spell out the letter “Y” when the optimal solution was found. In the problem with 10×10 Ising spin lattice, the number of combinations is to be 2^{100}, or approximately 10^{30}. Figs. 1(a)-(c) show spin states during the process of solving the max cut problem. First, the spin states are starting out randomly (Fig. 1(a)). Then, the letter begins to appear amid a certain amount of noise (Fig. 1(b)). Finally, “Y” appears very clearly without noise (Fig. 1(c)), and the global minimum for this problem is certainly achieved. Therefore, it is suggested that the optimal solution to the combinatorial optimization problems could be obtained using Ising computing architecture implemented on FPGA.



Figs.1 (a) - (c) Spin status transitions when solving a combinatorial optimization problem using Ising computer implemented on FPGA.

References

[1] S. G. Brush et al., Rev. Mod. Phys. 39 (1967) 883.
[2] M. W. Johnson et al., Nature 473 (2011) 194.
[3] M. Yamaoka et al., IEEE J. Solid – St. Circ. 51 (2016) 303.