Spin-dependent transport and current modulation in a current-in-plane spin-valve field-effect transistor

○(D2)Toshiki Kanaki[1], Tomohiro Koyama[2], Daichi Chiba[2], Shinobu Ohya[1,3], and Masaaki Tanaka[1,3]

[1]*Department of Electrical Engineering and Information Systems, The University of Tokyo,*

[2]*Department of Applied Physics, The University of Tokyo,*

[3]*Center for Spintronics Research Network, The University Tokyo*

E-mail: kanaki@cryst.t.u-tokyo.ac.jp

A spin metal-oxide semiconductor field-effect transistor (spin MOSFET), in which the source and drain electrodes are composed of ferromagnetic materials, has been intensively studied, aiming at future electronics applications [1,2]. Some experimental demonstrations of lateral and vertical spin MOSFETs have been reported thus far [3-6]; however, for both lateral and vertical spin MOSFETs, there still remain problems to overcome towards practical applications in the present status.

Here, we propose an alternative device, a current-in-plane spin-valve field-effect transistor (CIP-SV-FET), which comprises a ferromagnet / nonmagnet / ferromagnet trilayer and a gate electrode as shown in Fig. 1(a). This device can offer a functionality similar to that of spin MOSFETs due to the spin-valve effect and current modulation using a gate electric field. Also, the device performance is not affected by spin relaxation in the channel transport, which is a crucial issue in spin MOSFETs.

We fabricated a ferromagnetic-semiconductor GaMnAs-based CIP-SV-FET. The trilayer structure was grown on a lattice-relaxed $In_{0.17}Al_{0.83}As$ buffer layer [Fig. 1(b)], and thus the magnetic easy axes of the GaMnAs layers are perpendicular to the film plane. We measured the Hall resistance (R_{Hall}) and sheet resistance (R_{sheet}) under an external magnetic field $\mu_0 H$ applied perpendicular to the film plane. As shown in Figs. 1(c) and 1(d), R_{sheet} was modulated both by the magnetization configuration through the spin-valve effect (0.17%) and by the gate voltage (14%) at 36 K. Furthermore, we successfully demonstrated electric-field-assisted magnetization reversal of the upper GaMnAs layer [7].

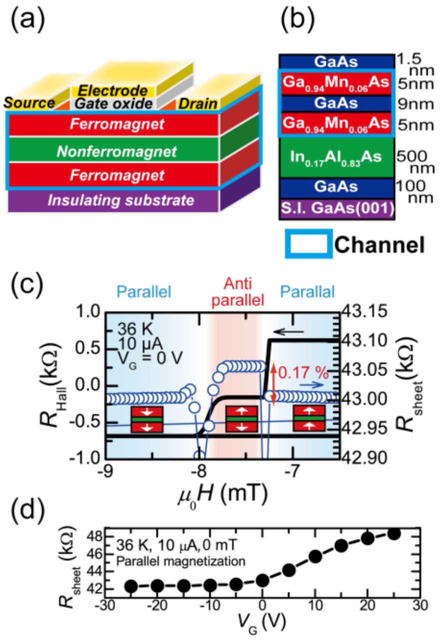

FIG. 1. (a)(b) Schematics of the current-in-plane spin-valve field-effect transistor (CIP-SV-FET) (a) and the heterostructure used in this study (b). (c) R_{Hall} (solid curve, left axis) and R_{sheet} (circles, right axis) *vs.* $\mu_0 H$. The gate voltage V_G is 0 V. (d) R_{sheet} *vs.* V_G. All data were taken with a bias current of 10 μA at 36 K.

This work was supported by Grants-in-Aid for Scientific Research, the Project for Developing Innovation Systems of MEXT, and Spintronics Research Network of Japan. Part of this work was carried out under the Cooperative Research Project Program of RIEC, Tohoku University. T. Kanaki acknowledges the financial support from JSPS through the Program for Leading Graduate Schools (MERIT).

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