Improvement of physical and electrical properties in SiC-MOS devices using deposited insulators on barium-enhanced thermal oxides

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Silicon carbide (SiC) has been proposed to be a promising wide bandgap semiconductor that can be employed instead of silicon (Si) for next-generation power devices. However, thermal oxidation of SiC requires higher temperatures (> 1100°C) than that of Si to grow thick oxide layers. Moreover, SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) using the thermal oxide as a gate insulator show low channel mobility (<8 $cm^2/V{\cdot}s$) due to defects at SiO_2/SiC interfaces. Lichtenwalner *et al.* recently reported that employing a thin barium (Ba) interface layer on the SiC substrate followed by oxidation with a deposited SiO_2 cap increases field effect mobility (μ_{FE}) up to 110 $cm^2/V{\cdot}s$, regardless of poor oxide breakdown properties [1]. We also investigated oxidation rate enhancement using Ba at 950°C in pure oxygen (O_2) ambient, so-called metal-enhanced oxidation (MEO) on SiC surfaces without any SiO_2 cap, and revealed that severe surface roughening is caused by Ba-MEO [2]. In this study, we further explored MEO for 4H-SiC systems with and without deposited insulator cap by means of physical and electrical characterizations.

After wet cleaning of 4H-SiC(0001) substrates with *n*-type epilayers, 0.5-nm-thick Ba layers were deposited on the substrates using the Knudsen cell. As illustrated in Fig. 1, some samples were selected to form a 45-nm-thick SiO_2 cap on the Ba surfaces using plasma-enhanced chemical vapor deposition (CVD). Then, all samples were oxidized immediately in high-purity O_2 gas at 950°C for 4 h.

We observed substantial increases in the oxide thickness using spectroscopic ellipsometry for both samples with Ba. While 67-nm-thick SiO_2 layer was formed by Ba-MEO without capping, the samples with a deposited CVD-SiO_2 cap showed extra 86-nm-thick SiO_2 layer growth on the SiC substrate. Also, as shown in Fig. 1, the atomic force microscopy (AFM) images of these samples exhibited different surface morphologies, in which no grain was found and the reduced RMS roughness for the sample with the capping layer.

Next, the electrical properties were examined for SiC-MOS capacitors fabricated by depositing circular Al gate electrodes on top of the oxides. As shown in Fig. 2(a), the energy distributions of interface state density (D_{it}) were estimated based on the high-low method that compares 1 MHz and quasi-static capacitance–voltage curves. All samples with MEO showed D_{it} reductions compared with the reference capacitor with conventional dry oxidation at 1150°C for 4 h (dry ox.). Also, the capacitors containing CVD-SiO_2 cap showed slightly better interface quality than those capacitors with only MEO-SiO_2. Figure 2(b) shows oxide leakage and breakdown characteristics. It is found that the leakage current in the MEO sample exponentially increased at the oxide field around 1.5 MV/cm probably due to defect centers in SiO_2 caused by Ba. In contrast, the sample with CVD-SiO_2 capped MEO shifted the leakage to the higher field above 3 MV/cm, indicating that well-defined capping layers are essential for gate reliability improvement in the Ba-MEO SiC-MOS devices.

[1] D. J. Lichtenwalner *et al.*, Mater. Sci. Forum **858**, 671 (2016).
[2] A. Chanthaphan *et al.*, 63rd JSAP Spring Meeting, **20p-H101-12**.

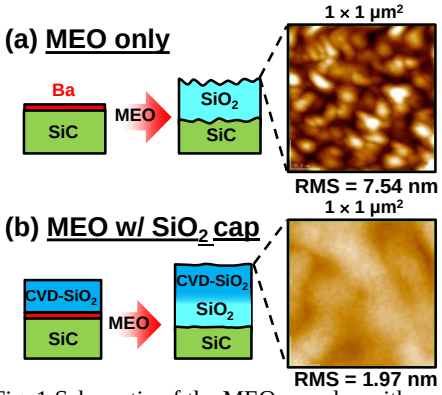

Fig. 1 Schematic of the MEO samples with and without CVD-SiO_2 cap and their AFM images (1×1 μm^2) of the uppermost oxide surfaces.

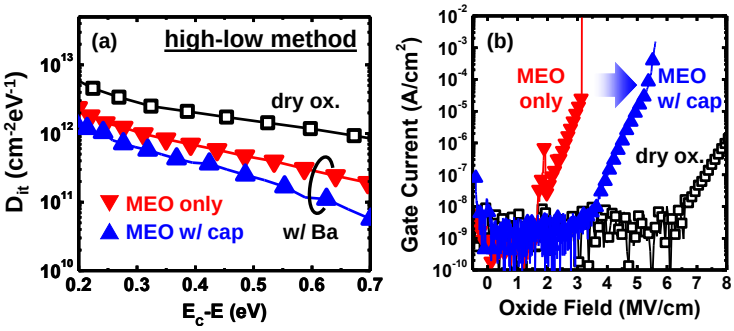

Fig. 2 (a) Energy distribution of D_{it}, and (b) J–E characteristics for the capacitors containing oxides formed by MEO with and without insulator capping (closed symbols) and the reference capacitor without Ba (dry ox.).