Computational nano OPC DFM for LV Fin-type SRAM

Kazuya Kadota
Nanoscience Lab.,
E-Mail: drkadota@hotmail.co.jp

Design For Manufacturing (DFM) where the state-of-the-art nano-devices of the sub-20nm node to a subject, for each of the technology has been intricately sophisticated, comprehensive optimization to predict the performance of the device came become very important.

To get effective solutions on these subjects, one of the lithographic key is a nano Optical Proximity Correction (OPC) control with SMO technology, and another is Total Computer Aided Design (TCAD) approach using the most advanced computer simulations. And, it is very important to obtain DFM solutions by integrating both.

On the other hand, to meet the needs of low-voltage drive and the characteristic variation reduction, in order to obtain a state-of-the-art device performance, the Fin-type transistors are introduced globally as the mainstream because of wider process control margin.

This paper, from the point of view of the sub-20nm node DFM, the computer simulation are conducted on ArF immersion exposure technology with SMO in Single Patterning Technology (SPT) and Quadruple Patterning Technology (QPT) , and the guideline of design rules are obtained after the OPC optimization.

Furthermore, the simulated transistor pattern shape are directly migrated into the TCAD process flow.

Then calculated I-V characteristics on 6 transistors configuration under the various process and device parameters on TCAD tool, and finally summarized Static Noise Margin (SNM) of SRAMs as one of the most extensively used design guideline of Microprocessors and Logics. Here, various parameters that determine the performance of SRAMs (Fin width, height, angle, dopant concentrations, electric field strength, work function, drive voltage, and operation speed) are intentionally varied on the TCAD, and calculated the I-V characteristics of each transistor .

In this study, Tachyon™ and HyENEXSS™ were used for lithography and device as the most advanced computer simulation tools, respectively.

Figure shows one of the pseudo rectangular shape results on Quadruple Patterning Technology (QPT) simulation, but the overlay error of intentionally X direction to ± 12nm was generated in this case,

When operate these results at very low driving voltage (0.4V) on the TCAD simulation, SRAM characteristics (SNM) are shown very good balanced performance to meet the DFM goal.

This computational method is highly sophisticated DFM technology to predict for the cutting-edge nano-devices toward for the sub-20nm nodes era.

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Fig.1 and 2: DFM Computational Flow (Left) and SNM Prediction (Right) by QPT Lithography extend on Overlay Error Margin.