Effect of Gate Dielectrics on Trap Density in PbS Nanocrystal Field-Effect Transistors
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PbS colloidal nanocrystals (CNCs) are of high interest for optoelectronics because of their solution processability, band gap tunability, and high absorbance.\textsuperscript{[1]} As active materials for field-effect transistors (FETs), the PbS/gate dielectric interface is able to introduce as well as influence carrier traps, which lead to low charge carrier mobility. Here, we report the study of the effect of gate dielectric properties on the carrier traps in PbS NC-FETs by treating the oxide dielectric with self-assembled monolayers (SAMs) as well as by utilizing several polymer dielectrics with different dielectric constants.

The SiO\textsubscript{2} dielectric with pre-patterned Au electrode was treated with hexamethyldisilazane (HMDS), on which PbS semiconducting thin film was then spin-coated. To improve the film conductivity, the film was soaked in the solution of short thiol-based ligands which replaces the long oleic acid ligands on the NC surfaces. The solutions of various polymers with dielectric constant range of 2.1-40 were spin-coated on the PbS film as top gate dielectrics with evaporated Al as gate electrode. HMDS treatment reduces electron trap density of states (DOS) by passivating the silanol groups on the SiO\textsubscript{2} surfaces which act as electron trapping site, as indicated in Figure 1(a). This reduction in the trap DOS results in improvement in electron mobility up to 0.07 cm\textsuperscript{2}V\textsuperscript{-1}s\textsuperscript{-1}, a factor of 3 higher than that in bare SiO\textsubscript{2}-gated devices. The use of hydroxyl-free gate dielectrics, Cytop polymer, further reduces the trap DOS for both electrons and holes by a factor of two. This, in turn, leads to an increase in electron mobility up to 0.2 cm\textsuperscript{2}V\textsuperscript{-1}s\textsuperscript{-1}. Furthermore, we observe that the dielectric constant of gate dielectrics can influence the trap DOS in the devices. Obviously, the DOS of deep traps in PbS NC-FETs increases with increasing the dielectric constant of gate dielectrics as displayed in Figure 1(b), which can be attributed to the broadening of the trap DOS. This broadening can be caused by strong interaction between trapped carriers and the polarization of dielectrics at the PbS/dielectric interfaces, which is able to change the depth of trap states.


Fig. 1 (a) Trap DOS in PbS FETs with SiO\textsubscript{2} and Cytop dielectrics. (b) DOS of deep electron traps as a function of dielectric constant.