縦型スピン電気二重層トランジスタ

Vertical spin electric double layer transistor

◦寺田 博、レ デゥック アイン、大矢 忍、岩佐 義宏、田中 雅明 (東大院工)
◦Hiroshi Terada, Le Duc Anh, Shinobu Ohya, Yoshihiro Iwasa, and Masaaki Tanaka
(Graduate School of Engineering, The University of Tokyo)
E-mail: terada@cryst.t.u-tokyo.ac.jp

A spin metal-oxide-semiconductor field-effect transistor (spin MOSFET [1]) is one of the promising devices for future electronics. In the spin MOSFET, the drain-source current I_{DS} is modulated by both electric field and magnetization configurations. In previous studies, conventional planer spin MOSFET devices have been studied; however, the magnetoresistance (MR) ratios were very small (0.03% [2], 0.005% [3]). Recently, we have proposed a *vertical* spin MOSFET structure composed of epitaxially grown very thin channel sandwiched between ferromagnetic source/drain, which is preferable for the spin-dependent transport [4]. In our previous study [4], I_{DS} was modulated by 60% with MR and was modulated by 0.5% with a gate electric field. In this study, to obtain a larger I_{DS} modulation ratio, we fabricated a vertical spin electric double layer transistor (vertical spin EDLT) structure, which consists of GaMnAs-based mesa diodes, a gate electrode, and ionic liquid, as shown in Fig. 1(a). We reduced the size of the device compared with the one in our previous study to decrease the leak current which flows deeply inside from the surface of the mesas where the modulation of the potential with a gate electric field is weak. In addition, we applied the gate electric field by using ionic liquid, which is preferable to apply higher electric field.

We grew a heterostructure composed of $Ga_{0.95}Mn_{0.05}As$ (9.2 nm)/ GaAs (11 nm)/ $Ga_{0.95}Mn_{0.05}As$ (10 nm)/ GaAs: Be (100 nm) on a p^+ GaAs (001) substrate by low-temperature molecular beam epitaxy. After the growth, we fabricated elongated shaped mesas with the size of 500 nm × 50 μm and the comb-shaped drain electrode which is connected to the top of the thirty mesa diodes, as shown in Fig. 1(a). The substrate was used as a source electrode. The gate electrode was deposited on the insulating film placed beside the mesa diodes. The gate electrode and the mesa diodes were covered with electrolyte (DEME-TFSI). By applying a gate-source voltage V_{GS}, the potential at the surface of the mesas is modulated. As a result, I_{DS} is modulated by V_{GS}. As shown in Fig. 1(b), the obtained I_{DS} decreased with increasing V_{GS}, and the modulation ratio $\{I_{DS}\ (V_{GS} = -3\ V) - I_{DS}\ (V_{GS} = 0\ V)\}/I_{DS}\ (V_{GS} = 0\ V)$ reaches 17.6% when V_{DS} = 10 mV, at 3.8 K. This is much higher than that obtained in the previous report on the vertical spin-MOSFET. We measured the tunnel magnetoresistance (TMR) varying the in-plane magnetic field angle (Figs. 1(c) and 1(d)). We found unexpected behavior that the anisotropy of the TMR (i.e. the shape of the pattern in Figs. 1(c) and 1(d)) changes with V_{GS}. In the presentation, we discuss the origin of the change of the magnetic anisotropy induced by the gate electric field.

This work was partly supported by Grants-in-Aid for Scientific Research, Project for Developing Innovation Systems of MEXT.

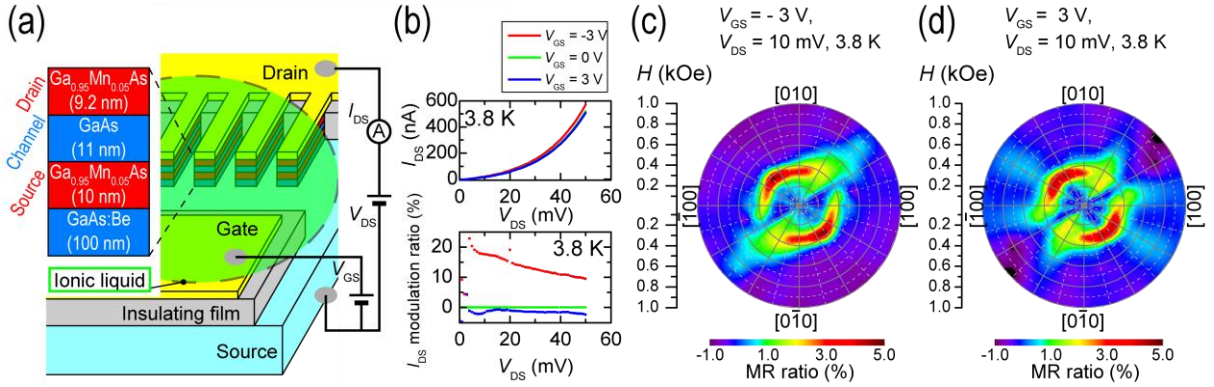

Figure 1(a) Schematic illustration of the device structure. (b) I_{DS}-V_{DS} characteristics at V_{GS} of -3 V, 0 V, and 3 V. (c) (d) Color contour plot of the TMR with the various in-plane magnetic field directions (at V_{DS} = 10 mV) at V_{GS} = -3 V (c) and at V_{GS} = 3 V (d). All data were obtained at 3.8 K.

[1] S. Sugahara and M. Tanaka, Appl. Phys. Lett. **84**, 2347 (2004). [2] R. Nakane, T. Harada, K. Sugiura, and M. Tanaka, Jpn. J. Appl. Phys. **49**, 113001 (2010). [3] T. Sasaki *et al.*, Phys. Rev. Applied **2**, 034005 (2014). [4] T. Kanaki, H. Asahara, S. Ohya, and M. Tanaka, Appl. Phys. Lett. **107**, 242201 (2015).