P チャネル InGaN/GaN ヘテロ構造金属酸化物半導体電界効果トランジスタ P-Channel InGaN/GaN heterostructure metal-oxide-semiconductor field effect transistor based on polarization-induced two-dimensional hole gas

 桑 立雯^{1,2}、張 克雄¹、角谷 正友¹、廖 梅勇¹、小出 康夫¹

 1.物質材料研究機構 2. JST-PRESTO

Liwen Sang^{1,2}*, Kexiong Zhang¹, Masatomo Sumiya¹, Meiyong Liao¹, Yasuo Koide¹, and

Liwen Sang

¹National Institute for Materials Science, ²JST-PRESTO.

*e-mail: <u>SANG.Liwen@nims.go.jp</u>

The conventional Si-based complementary logic integrated circuits (ICs) show the drawbacks of large leakage current and poor reliability in harsh environments. Wide-bandgap semiconductor III-Nitrides provide a better choice for the logic ICs applications owing to their superior physical and chemical properties. To achieve the complementary ICs, both n- and p-channel FETs with well-matched performance are necessary. Recently, III-Nitrides n-channel heterojunction FETs using polarization-induced two-dimensional electron gas (2DEG) have already been extensively investigated with lower specific on-resistance and higher electron mobility compared with those of Si-based FETs. However, little attention has been paid to p-channel FETs because of the difficulty in obtaining hole with high charge density and high mobility. It has been theoretically simulated that for the compressively strained InGaN layer on the relaxed GaN template, holes can be confined close to the lower interface as a result of the dominant piezoelectric polarization field. But it is still difficult to experimentally extract high-density 2DHG in the InGaN system.

In this paper, a super-thin ultra-flat GaN spacer layer is proposed between InGaN and high-resistance GaN template to reduce the interface roughness scattering for the 2DHG. With the optimized structure for a high-density 2DHG at InGaN/GaN heterojunction, a MOSFET using Al_2O_3 as gate dielectric is demonstrated for the first time (Fig. 1). The accumulation of 2DHG with high concentration at the lower interface of InGaN/GaN is confirmed from both theoretical simulation and capacitance-voltage (C-V) measurement. The MOSFET shows a high drain-source current IDS of 0.51 mA/mm at the gate voltage V_{GS} of -2 V and drain bias V_{DS} of -15 V, and ON/OFF ratio of two orders of magnitude at room temperature. The normal operation of MOSFET at 8 K further proves that the p-channel behavior is originated from the polarization-induced 2DHG.



Figure. 1 Calculated band diagram and output characteristic of InGaN/GaN MOSFET

References

1. Kexiong Zhang, Masatomo Sumiya, Meiyong Liao, Yasuo Koide, and Liwen Sang, submitted (2016)