Triple Gate Graphene Nanoribbon Field Effect Transistor (TG-GNRFET)

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Tunnel Field Effect Transistors (TFETs) attract much interest of the scientific community as a promising alternative for MOSFETs. Low off current and small sub-threshold slope are their major advantages. However, the on current is currently much lower than that for MOSFETs. Therefore, ways to increase the on current are actively investigated. According to quantum mechanics, materials with a small band gap and small effective mass of charge carrier can show higher band-to-band tunnel current. It is therefore expected that with their massless Dirac fermions and tunable bandgap, graphene is one of the most suitable candidates for TFETs. In this direction, we previously introduced the double gate GNR that showed a slight band-to-band tunnel current contribution to the total current[1]. In this work we propose a triple gate GNR field effect transistor (TG-GNRFET)(see Fig.1).

First, numerical simulation was done by using the three-dimensional device simulator (Silvaco ATLAS) to investigate the gate-induced potential distribution. Triple-gate devices show a potential stepper profile (see Fig.2) than the double gate structure with a back gate. Based on this design simulation, the TG-GNRFET was fabricated using oxygen plasma etching and conventional lift-off technique. For that purpose, high-resolution negative tone resists (HSQ) and positive tone resists (SML) were used as etch mask and lift-off resist, respectively (Fig.3). The Separation gap between the central gate (TG2) and the outer gates (TG1 and TG3) plays a crucial role in controlling the potential profile shape (see Fig.2) which affect the tunneling probability. Therefore, devices with different separation gap were fabricated to investigate this effect (Fig.3). Device characteristics are investigated and will be presented at the conference.

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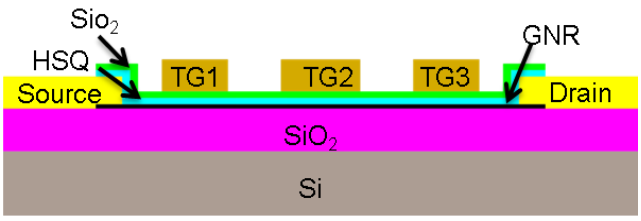

Fig.1: Schematic cross- sectional view of the triple top gate Transistor

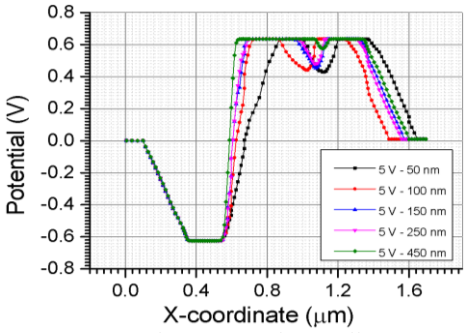

Fig.2: Simulation of potential profile at different middle gate length

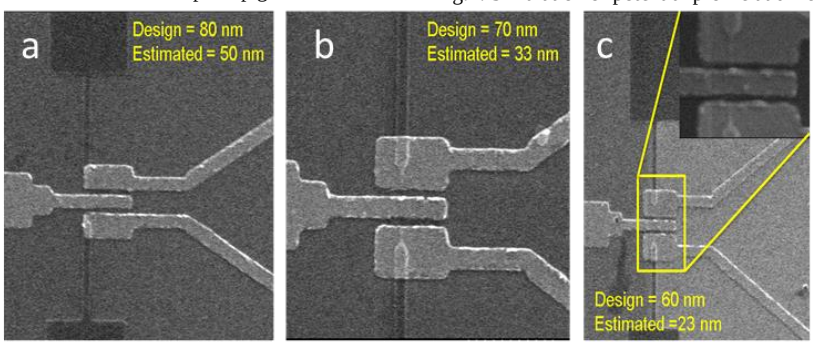

Fig.3:SEM image of the triple top gate devices with different separation gap

References:

[1]Ahmed Hammam *et al.*, The 76th JSAP Autumn Meeting, 2015