Field-Plated Ga_2O_3 MOSFETs With a Breakdown Voltage of Over 750 V

National Institute of Information and Communications Technology[1], Tamura Corporation[2]

°Man Hoi Wong[1], Kohei Sasaki[2,1], Akito Kuramata[2], Shigenobu Yamakoshi[2], Masataka Higashiwaki[1]

E-mail: mhwong@nict.go.jp

This work presents the first demonstration of single-crystal Ga_2O_3 metal-oxide-semiconductor field effect transistors (MOSFETs) with a field plate (FP) for enhanced off-state breakdown voltage (V_{br}). A SiO_2 dielectric was used to serve a dual functionality for FP mechanical support as well as device passivation. The high resistivity of unintentionally-doped (UID) Ga_2O_3 grown by molecular beam epitaxy (MBE) was harnessed for planar device isolation without mesa etching. The FP-MOSFETs exhibited a V_{br} of 755 V, a drain current (I_{DS}) on/off ratio of over 10^9, and stable high temperature operation against 300°C thermal stress.

Figure 1 shows a schematic of the MBE-grown Ga_2O_3 FP-MOSFET. The *n*-type channel and source/drain ohmic contacts were formed by Si ion implantation doping. Based on Silvaco ATLAS device simulations, a 0.4-μm-tall FP extended 2.5 μm toward the drain was adopted for balanced peak off-state electric fields at the drain edges of the gate (position × in Fig. 1) and of the FP (position * in Fig. 1) without excessive charge depletion by the FP. The gate electrode was fabricated by a highly selective SiO_2 dry etch process followed by self-aligned metal deposition. The FP was then realigned to the exposed gate electrode.

The UID Ga_2O_3 provided effective inter-device isolation with a high resistivity of 10^8 – 10^9 Ω-cm. At room temperature (RT), the FP-MOSFET delivered a maximum I_{DS} of 78 mA/mm at a gate voltage (V_{GS}) of +4 V (Fig. 2). The three-terminal off-state V_{br} of 755 V at V_{GS}=-55 V was an improvement of more than 80% over the previously reported value (Fig. 2) [1]. Current surge upon destructive breakdown occurred between source and drain, which could be associated with punch-through in Ga_2O_3 or failure of the unoptimized SiO_2 dielectric. The intrinsic V_{br} of the device – being determined by field peaks in the gate-drain depletion region – would therefore have exceeded the experimental V_{br} as to be expected from the simulations. I_{DS} on/off ratios exceeding 10^9 and 10^3 were achieved at RT and 300°C, respectively, at a drain voltage (V_{DS}) of 30 V (Fig. 3). Pulsed I_{DS}-V_{DS} measurements performed at an off-state quiescent drain/gate bias condition of (V_{DQ}, V_{GQ}) = (40 V, -36 V) with 100-μs pulse width and 0.1% duty cycle showed no current collapse, attesting to effective passivation of surface traps and high Ga_2O_3 material quality.

This work was partially supported by Council for Science, Technology and Innovation (CSTI), Cross-ministerial Strategic Innovation Promotion Program (SIP), “Next-generation power electronics” (funding agency: NEDO).

[1] M. Higashiwaki *et al.*, Tech. Dig. IEEE Int. Electron Devices Meet., pp. 28.7.1 – 4 (2013).

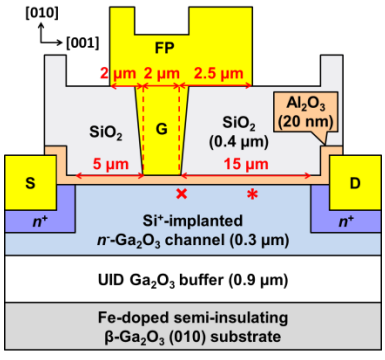

Fig. 1. Schematic cross section of the Ga_2O_3 FP-MOSFET. The × and * symbols indicate positions of peak off-state electric fields in the Ga_2O_3 channel.

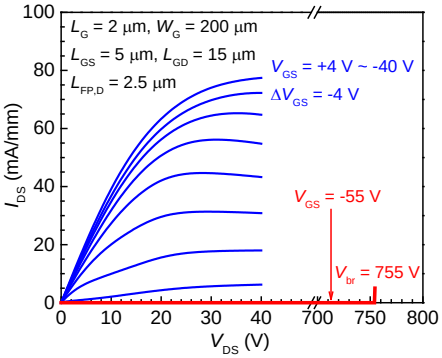

Fig. 2. DC output characteristics and off-state breakdown curve of the Ga_2O_3 FP-MOSFET.

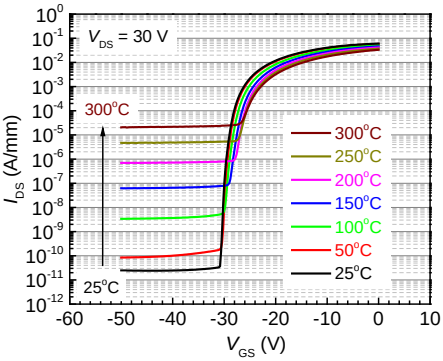

Fig. 3. Temperature-dependent transfer characteristics of the Ga_2O_3 FP-MOSFET at V_{DS}=30 V showing normal device operation from RT to 300°C.