Near-interface border traps characterization for GeO_2/Ge gate stacks grown by low and high temperature thermal oxidation by using deep-level transient spectroscopy

Wei-Chen Wen[1], Taisei Sakaguchi[1], Keisuke Yamamoto[1], Dong Wang[1] and Hiroshi Nakashima[2]

[1] Interdisciplinary Graduate School of Engineering Sciences, Kyushu Univ.

[2] Global Innovation Center, Kyushu Univ.

E-mail: 2ES15222P@s.kyushu-u.ac.jp

Introduction A high-quality gate-stack formation on Ge is essential for high-performance Ge MOSFETs. Although a GeO_2 is effective in reducing the interface-traps (ITs), a large amount of border-traps (BTs) causes serious problems. In this study, we established a method of BT characterization by deep-level transient spectroscopy (DLTS), and investigated BTs in two kinds of MOS capacitors (CAPs) with a structure of SiO_2/GeO_2/Ge. One was a relatively thick GeO_2 by thermal oxidation at 550°C, at which GeO_2 volatilization may occur at the GeO_2/Ge interface [1]. The other was a thin GeO_2 by the oxidation at 425°C, at which the volatilization may not occur. The Al post metallization annealing (PMA) effect on BT passivation was also studied.

Experimental After substrate cleaning, 1 nm-SiO_2/1 nm-GeO_2 bilayer passivation was performed [2], followed by a post thermal oxidation (PTO) at 550°C for 15 min or 425°C for 9 h in O_2 ambient. Next, 14-nm-thick SiO_2 was deposited on the both samples, followed by a post deposition annealing at 400°C for 30 min in N_2. Then, an Al gate film was deposited on the SiO_2 surface by thermal evaporation. Before electrodes formation, an optional Al-PMA was carried out at 300°C for 30 min in N_2. The equivalent oxide thicknesses (EOTs) of the MOSCAPs with PTO at 550 and 425°C were ~19.5 and 16.8 nm, corresponding to GeO_2 thicknesses of 6.6 and 2.6 nm, respectively.

DLTS measurements were performed using a lock-in integrator. Pulse frequency f=10 Hz were used, which corresponds to BT position z_0=1.4 nm from the interface for p-MOS and z_0=2.0 nm for n-MOS.

Results and discussion Figure 1 shows DLTS signal intensity (I_{DLTS}) dependence on pulse height (V_P) with a maximum t_w of 5 ms at different temperatures (Ts) for a MOSCAP with PTO at 550°C and without Al-PMA. Let us pick up the result at 80 K as an example. The I_{DLTS} drastically increased when the V_P increased from 0 to 0.5 V. Note 0.5 V is approximately the V_{FB} at 80 K for this sample. Therefore, this increase is dominated by the capture process of IT [3]. We believe that the weakest injection condition (t_w=2 μs) under pulse intensity E_{AP}=0 MV/cm is enough to compose the IT signals. (E_{AP} =V_{AP}/EOT, where V_{AP} is the applied voltage above flat band voltage.) Therefore, we use these data for IT density (D_{it}) calculation. In the case of V_P > 0.5 V, namely after the accumulation was established, the increase in I_{DLTS} with V_P > 0.5 V was governed by the capture process of BT because of an increase in hole numbers at Ge side of the GeO_2/Ge interface. After subtracting the IT signal from I_{DLTS}, we calculate the BT density (N_{bt}). The details will be presented in the conference.

D_{it} characteristics (not shown) are almost identical for both the MOSCAPs, implying that the interface property is not influenced by GeO_2 volatilization. The Al-PMA is effective in decreasing D_{it} near the valence band edge but not near the conduction band edge (even worse), which is consistent with our previous experimental results of Al-PMA effects on Ge-MOSFET performance [3, 4].

Figures 2(a) and 2(b) show dependence of N_{bt} on T for p-MOSCAPs with PTO at 550 and 425°C, respectively. It was confirmed from these results that 1) the N_{bt} for p-MOS with 425°C-PTO is a half of that with 550°C-PTO under E_{AP}=2 MV/cm, suggesting BT in p-MOS is associated with GeO_2 volatilization; 2) the N_{bt} for p-MOS is drastically decreased by Al-PMA. The N_{bt}s for n-MOS with PTO at 425 and 550°C (not shown) are almost the same and not decreased by Al-PMA, suggesting the species of BT in n-MOS are different from that of p-MOS.

References [1] K. Prabhakaran *et al.*, Thin Solid Films **369**, 289 (2000) [2] K. Hirayama *et al.*, Solid State Electron. **60**, 122 (2011) [3] D. Wang *et al.*, J. of Appl. Phys. **112**, 083707 (2012) [4] Y. Nagatomi *et al.*, Mat. Sci. Semicond. Process. (2016), doi: *10.1016/j.mssp.2016.11.014*

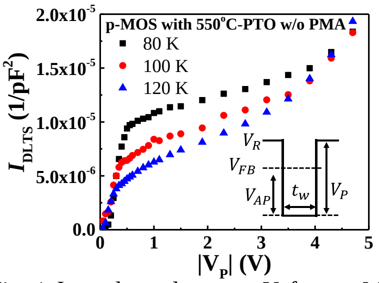

Fig. 1 I_{DLTS} dependence on V_P for a p-MOS with PTO at 550°C without Al-PMA.

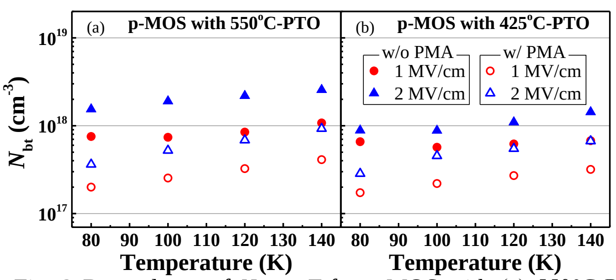

Fig. 2 Dependence of N_{bt} on T for p-MOS with (a) 550°C-PTO and (b) 425°C-PTO. The results with Al-PMA are also shown.