ALD $Al_2O_3/GeO_x/Ge$ 界面の電子と正孔に対する遅い準位の物理的起源に関する考察

Study on physical origins of slow traps for electrons and holes in ALD $Al_2O_3/GeO_x/Ge$ interfaces

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Introduction Ge is an attracting channel material for next generation MOSFETs because of the higher electron and hole mobility than Si. Here, the GeO_2/Ge structure is one of the most promising Ge surface passivation layers because a low interface trap density (D_{it}) has been expected [1-4]. As one of the realistic gate stacks, we have proposed and demonstrated high-k/GeO_x/Ge structures realized by plasma post oxidation (PPO), such as $Al_2O_3/GeO_x/Ge$ and $HfO_2/Al_2O_3/GeO_x/Ge$, which have been shown to have 1 nm or thinner equivalent oxidation thickness (EOT) and low D_{it} of ~10^{11} $eV^{-1}cm^{-2}$ [5, 6]. However, a large amount of slow traps included in these gate stacks is one of the remaining most critical issue [7-9].

While any defects in Al_2O_3 have been reported to be responsible for this slow trapping [9], we have recently found that the slow traps for electrons could exist inside GeO_x formed by PPO [10]. However, the physical origin of the slow trap generation for electrons and holes has not been understood yet. In this study, we systematically compare the slow trap density of electron and holes for the Al_2O_3/GeO_x/Ge interfaces with different GeO_x thickness prepared by post or pre plasma oxidation for ALD Al_2O_3/Ge stacks [11, 12].

Experiments N- and p-type **(**100) Ge wafers were cleaned by de-ionized water, acetone and HF. After this pre-cleaning, plasma pre- oxidation was performed by using ECR plasma of Ar (9 sccm) and O_2 (3 sccm) at 300 °C under 650 W RF power for 1-4 s to form GeO_x with the different thickness. Subsequently, 1.5 to 2.4-nm-thick Al_2O_3 was deposited at 300°C by ALD. Post deposition annealing (PDA) was performed for 30 min at 400 °C in N_2 ambient, followed by formation of 100-nm-thick Au gate electrodes and 100-nm-thick Al back contacts by thermal evaporation. The slow trap density (ΔN_{st}) is evaluated from hysteresis in the C-V sweep of the fabricated MOS capacitors as a function of the effective oxide field (E_{ox}). Here, E_{ox} and ΔN_{st} are determined by $E_{ox} = (V_G - V_{FB})/CET$ and $q\,\Delta N_{st} = C_{ox}\,\Delta V_{hys}$ [9].

Results and Discussions Fig. 1 shows ΔN_{st} of Al_2O_3(1.5 nm)/GeO_x/Ge with plasma pre-oxidation as a parameter of the GeO_x thickness. It is found that ΔN_{st} for holes in the Al_2O_3/GeO_x/p-Ge MOS interfaces has the GeO_x thickness variation, while ΔN_{st} for electrons in the Al_2O_3/GeO_x/n-Ge MOS interfaces has no dependence. This phenomenon indicates that slow traps for electrons and holes exist in different positions in the Al_2O_3/GeO_x/Ge MOS interfaces. Fig. 2 show a schematic diagram of possible locations of slow traps in the Al_2O_3/GeO_x/Ge MOS interfaces. The meaningful GeO_x thickness dependence and almost no Al_2O_3 thickness dependence of ΔN_{st} for the p-Ge MOS capacitors suggest that slow traps for holes can locate around the Al_2O_3/GeO_x interface. Also, the smaller hysteresis and smaller ΔN_{st} for the p-Ge capacitors indicate that slow trap density for holes is smaller than that for electrons. On the other hand, almost no GeO_x and Al_2O_3 thickness dependencies of ΔN_{st} for the n-Ge capacitors suggest that slow traps for electrons can locate near the GeO_x/Ge MOS interfaces. It is also found in Fig. 3 that ΔN_{st} of electrons is significantly higher for plasma post-oxidation than that for plasma pre-oxidation. This result indicates that slow traps near the Ge conduction band side are additionally generated during the PPO process. A possible origin of this slow trap generation during PPO is some reaction of Al_2O_3 and GeO_x, and/or inter-diffusion of Al and Ge. On the other hand, there is no additional traps generate during PPO near the Ge valence band side, as seen in Fig. 3.

Conclusion The main slow traps in the Al_2O_3/GeO_x/Ge interfaces can locate near the GeO_x/Ge interfaces for electrons and near the Al_2O_3/GeO_x interfaces for holes. It has been revealed that slow traps for electrons are additionally generated during the PPO process near conduction band side.

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References [1] D. Kuzum et al, EDL, 29 (2008)328 [2] H. Matsubara et al, APL, 93 (2008) 032104 [3] T. Sasada et al, JAP, 106 (2009) 073716 [4] Y. Fukuda et al, JJAP, 44 (2005) 7928 [5] R. Zhang et al, APL, 98 (2011) 112902 [6] R. Zhang et al, TED, 60 (2013) 927 [7] R. Zhang et al, IEDM, (2011) 642 [8] J. Franco et al, IEDM, (2013) 397 [9] G. Groeseneken et al, IEDM, (2014) 828 [10] M. Ke et al, APL, 109 (2016) 032101 [11] R. Zhang et al, JES, 158 (2011) 178 [12] L. Nyns et al, ECS Tran, 35 (2011) 465 [13] M. Ke et al, MEE, 147 (2015) 244.

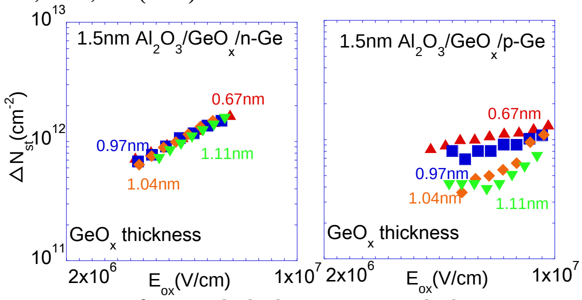

Fig.1: ΔN_{st} of 1.5-nm-thick Al_2O_3/GeO_x/Ge with plasma pre-oxidation time from 1 to 4s.

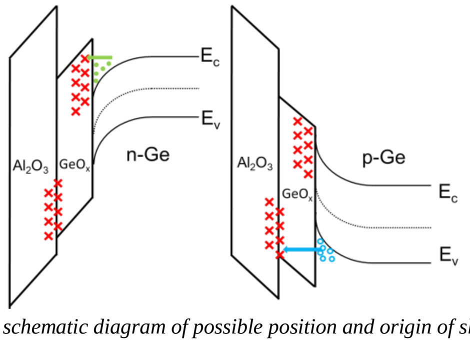

Fig.2: schematic diagram of possible position and origin of slow traps of 1.5-nm-thick Al_2O_3/1.04-nm-thick GeO_x/n- and p-Ge

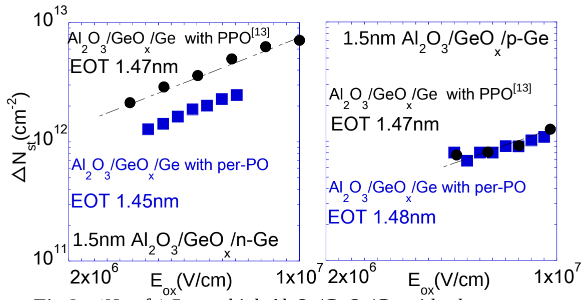

Fig.3: ΔN_{st} of 1.5-nm-thick Al_2O_3/GeO_x/Ge with plasma post or pre-oxidation with an EOT ~1.5-nm-thick