
Symposium (Oral) | Symposium | Science of impurity control in silicon wafers

[5p-A204-1~9]Science of impurity control in silicon wafers

Toshiaki Ono(SUMCO), Hiroaki Kariyazaki(GWJ)

Tue. Sep 5, 2017 1:30 PM - 5:45 PM A204 (204)

△：奨励賞エントリー

▲：英語発表

▼：奨励賞エントリーかつ英語発表

空欄：どちらもなし

1:30 PM - 2:00 PM

[5p-A204-1]Recent gettering technology trends for silicon devices from device engineering perspective

OKensuke Okonogi¹ (1.Micron Memory Japan)

Keywords:Gettering

Depending on the requirements of portable electronic devices, current advanced memory devices have a minimum feature size of 10 nm scale. Chip stack technology such as Through Silicon Via (TSV) process has been developed to increase capacity and multifunctionality. These state-of-the-art technologies also require optimal crystallinity for silicon wafers. Based on the trend of silicon wafers for DRAM and grasping current problems from technical papers, I would like to discuss future gettering development.