Multi-Layer All Sol-Gel Fabrication Technique on Bulk Silicon toward Vertical Coupler

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I. Introduction

Space division multiplexing (SDM) [1] is a technique that is proposed as one of the main candidate to address the issue of ever increasing demand for greater data transmission. Multi-core fibres (MCF) are a major component in realizing SDM to improve the capacity of data transmission bandwidth [2]. Because an MCF has a 3-dimensional core layout at the fibre facet, issues arise when coupling to MCF from planar photonic circuits such as optical switches, multiplexers, and waveguides. In order to address the coupling issue, a vertical coupled waveguide is an attractive solution [3]. In this work, we propose and fabricate a stacked multi-layer all sol-gel fabrication technique using ZnO and SiO_2 sol-gel on bulk Si to enable the realization of a vertical coupled waveguide.

II. Issues in Sol-gel Multilayer Fabrication

The prepared SiO_2 sol-gel solution was coated onto Si by a spin-coater and then heating was performed by a thermal annealer. Heating and cooling profile is shown in Fig.1. However, deformation (crack) was appeared on SiO_2 sol-gel layer due to stress during the cooling down stages. No crack was looked during the heating up stage because SiO_2 layer is still not fully cured yet. As a result, no stress on SiO_2 layer up to the maximum heating up temperature. Cracks were only observed (Fig.2) when cooling the sample from the maximum annealing temperature down to room temperature. During the cooling down stage, thermal stress that was generated and accumulated in SiO_2 layer is released and due to the thermal coefficient difference between SiO_2 and Si gives rise to the formation of cracks. Fig. 2(a) shows multiple oriented cracks and delamination of the SiO_2 sol-gel layer when cooling down at a rate of 8°C/min that appears over the whole sample. Slowing the cooling rate down to 4°C/min in Fig. 2(b) produces lesser cracks which still occurs over the whole sample but no delamination was observed. In Fig. 2(c), a rate of 2°C/min results only zig-zag cracks that originate from point defects on SiO_2 surface and is significantly less than the previous two cases. Finally, Fig. 2(d) with a rate of 1°C/min gives no cracks on the surface even ones originated from point defects.

III. Results and Discussion

The formation of cracks however can be reduced by controlling the cooling down ramp of the SiO_2 layer. The fabricated device is shown in Fig.3 with the thickness of each layers. Thermal annealing was done in order to densify all the sol-gel layers. All of the thickness were measured after the high temperature annealing process was effectively completed.

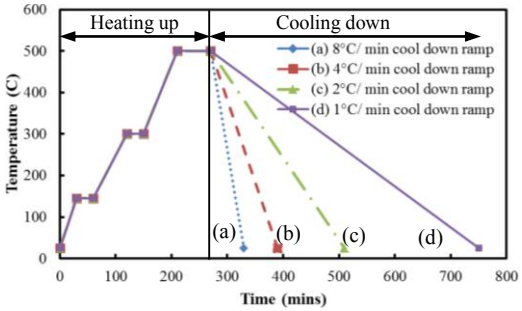

Fig. 1. Annealing profile for SiO_2 heating and cooling

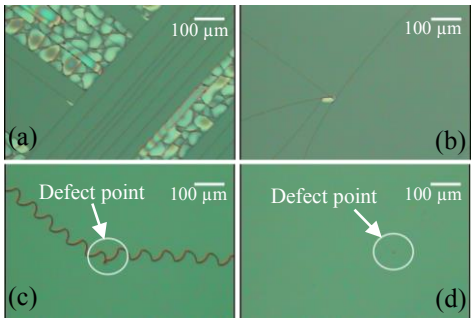

Fig. 2. Cracks on SiO_2 sol-gel surface with cooling down at (a) 8°C/min, (b) 4°C/min, (c) 2°C/min, and (d) 1°C/min

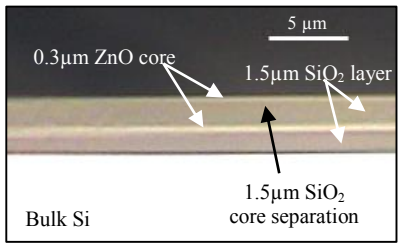

Fig. 3. Stacked multiple layers on bulk Si

IV. Conclusion

We have successfully stacked multiple layers by all sol-gel based fabrication technique. The capability to stack ZnO core layer and SiO_2 core separation layers on bulk Si with accurate thickness control enables the realization of vertical coupling.

References:

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[3] Y. Kokubun et al., IEEE J. Sel. Top. Quantum Electron, 11 (2005).