Band tail interface states and quantum capacitance in monolayer MoS_2 FET

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1. Introduction

MoS_2 FETs with high-*k* dielectrics have attracted much attention in ultimate scaled device research because of its natural thin body without dangling bonds ideally. However, both defects such as sulfur vacancy in MoS_2[1] and dangling bonds on the high-*k* oxide surface might severely degrade the MoS_2/high-*k* interface. In order to elucidate the underlying physical origin for the interface degradation, the *C-V* measurement is the powerful tool because the time constant and the energy distribution of interface states (D_{it}) can be determined[2-4]. However, unless quantum capacitance (C_Q) of monolayer MoS_2 is correctly extracted experimentally, the energy distribution of D_{it} cannot be determined. In this work, interface states are systematically evaluated as a function of E_F with the help of temperature-dependent C_Q extraction in order to elucidate the physical origin for the interface degradation.

2. Experimental

Monolayer MoS_2 FET with Ni/Au source/drain electrodes are fabricated by mechanically exfoliation technique on SiO_2 (90 nm)/n^+-Si substrate. Then, 1-nm Y metal was deposited via thermal evaporation at an Ar atmosphere of 10^{-1} Pa partial pressure, followed by oxidization at atmosphere to form buffer layer. The 10-nm Al_2O_3 oxide layer was deposited by atomic layer deposition before the Al top gate electrode formation.

3. Results & Discussion

As for *C-V* measurement of monolayer MoS_2 FET, the frequency dispersion is much reduced due to the relatively high crystallinity of bulk MoS_2 and the dedicated formation of Y_2O_3 buffer layer. **Fig. 1** shows C_Q extracted from the *C-V* measurement at 1 MHz assuming that interface traps are unable to respond to this frequency, with the theoretical model considering Fermi distribution and density of states (*DOS*) of 2D materials.[5] Experimental C_Q fits well with the theoretical curve at the wide range of V_{TG} (-1.8 ~ 0.1 V). While, interface traps cause the deviation from theoretical C_Q curve for the range of $C_Q < C_{it}$. In order to quantitatively evaluate D_{it}, the capacitance-frequency curves are measured at different V_{TG}. On the basis of equivalent circuit model, D_{it}, C_Q and time constant (τ_{it}) are extracted simultaneously by fitting experimental *C-f* curves as shown in **Fig. 2**. The inset in **Fig. 2** shows extracted C_Q and τ_{it}. Having confirmed the validity of C_Q theory, D_{it} is shown as a function of E_F as shown in **Fig. 3** by referring to theoretical C_Q-E_F correlation. The measured E_F range is extended to near the conduction band edge by low temperature measurements (75- 300 K). As a result, the tail-shape of D_{it} is clearly confirmed, which is different from that for bulk MoS_2.[3] This band-tail D_{it} will not be directly related with sulfur vacancies, because energy level for S vacancy[1] is slightly lower than the present energy range for D_{it}. The Mo-S bond bending due to the strain at the MoS_2/high-*k* interface or bond bending related with S vacancy might be the origin. Moreover, the important finding realized from this study is that ultra-thin 2D materials is more sensitive to the interface disorder because of reduced *DOS*, since the effect of interface traps on electrical properties is controlled by the relative magnitude of C_Q and C_{it}.

Acknowledgements This research was partly supported by the JSPS Core-to-Core Program, A. Advanced Research Networks, JSPS KAKENHI, Japan. **References** [1] H. Qiu *et al.*, Nat. Commun. 2013, **4**, 2642. [2] M. Takenaka, *et al.*, IEDM, 2016, 5.8.1. [3] W. Zhu, *et al.*, Nat. Commun. 2014, **5**, 1. [4] X. Chen *et al.*, Nat. Commun. 2015, **6**, 6088. [5] N. Ma *et al.*, 2D Materials 2015, **2**, 015003. [6] T. Sakurai *et al.*, J. Appl. Phys. 1981, **52**, 2889.

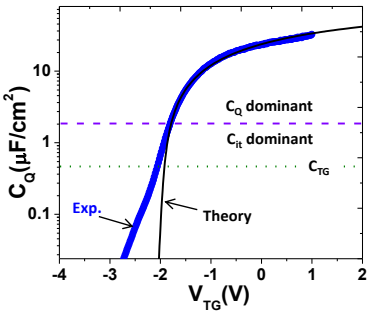

Fig. 1 C_Q-V_{TG} curves.

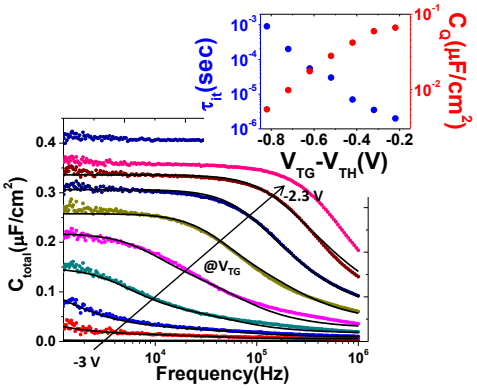

Fig. 2 *C-f* curves at different V_{TG}. Black lines are fitting curves. (Inset) τ_{it} and C_Q vs. V_{TG}-V_{TH}.

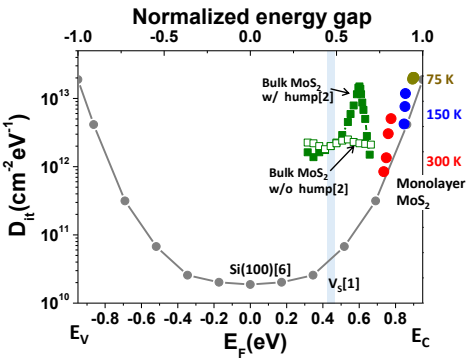

Fig. 3 D_{it} vs. E_F. Si(100)[6] and bulk MoS_2[2] are included by normalized E_G.