プラズマ酸化による酸化濃縮 GOI 層の薄膜化により作製した極薄ひずみ GOI pMOSFETs

Extremely-thin-body strained GOI pMOSFETs fabricated by thinning Ge condensation GOI through plasma oxidation

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【Background】 Ge has been considered as one of the most promising next generation CMOS channel materials, because the fundamental limitation of further scaling of Si MOSFETs is predicted in the near future. Moreover, ETB (extremely-thin-body) GOI (Ge-on-insulator) less than 10 nm is crucial as the geometry for suppressing short channel effects and lowering leakage currents. In addition, compressive strain application to ETB GOI layers can enhance pMOSFET performance. Among several GOI fabrication methods [1, 2], we have established the new Ge condensation method to form compressively strained GOI layers [3, 4]. However, ETB GOI pMOSFETs with high compressive strain has not been realized yet. In this study, strained GOI layers realized by the Ge condensation are thinned by ECR plasma oxidation. The operation of ETB strained GOI pMOSFETs with Ge thickness of 4.5 nm is demonstrated.

【Experiments】 Fig. 1 shows the process flow of UTB GOI layers with the Ge condensation process. Strained GOI layers were fabricated by Ge condensation process with reduced temperature cycles, as shown in Fig. 2. [3, 4, 5] The GOI layers were thinned down to 4.5 nm by repeating ECR plasma oxidation and etching of Ge oxides [6], as shown in Fig. 3. ECR plasma oxidation was done for 4, 6, 8 cycles and the thickness of thinned GOI layers were measured with ellipsometry. Also, the amout of strain was measured by Raman spectroscopy. Backgate operation GOI pMOSFETs were fabricated for relaxed and strained GOI layers.

【Results】Fig. 4 shows the Ge thickness of thinned GOI layers as a function of the oxidation cycle number. It is found that the GOI layer was digitally etched with an etching rate of 1.2 nm per each ECR plasma oxidation cycle. The 4, 6 and 8 cycles of the plasma oxidation realized the GOI thickness of 9.2, 6.7 and 4.5 nm, respectively. The TEM result shows the very uniform 4.5 nm-thick GOI layer, even with top-down process. Fig. 5 shows the strain of the thinned GOI layers. The amount of strain in the GOI thickness of 15, 9.2, 6.7 and 4.5 nm amount to 1.17, 1.18, 0.78 and 1.02 %, respectively. The thinning process by ECR plasma oxidation showed no relaxation of strain. As a result, we have successfully fabricated 4.5 nm-thick compressively strained GOI layer with 1.02 % strain. Note that the amount of strain in each GOI layers was different, due to the variation in initial SiGe-OI layers. Fig. 7 shows the I_d-V_g characteristics of the strained GOI layers thinned by plasma oxidation. While having not much degradation in on-current, off-current was dramatically lowered by thinning GOI. The on-off current ratio is shown in Fig. 8. The 4.5 nm-thick GOI pMOSFET showed extremely high on-off current ratio over 10^7, which is highest among GOI planar pMOSFETs reported so far and comparable even to device with fin geometry [7]. Fig. 9 shows the effective hole mobility of strained and relaxed GOI pMOSFETs with difference GOI thickness. The effective mobility of 15, 9.2, 6.7 and 4.5 nm-thick GOI pMOSFETs amount to 301, 265, 167 and 138 cm^2/Vs with strain of 1.17, 1.18, 0.78, and 1.02%, respectively. The enhancement factors of the corresponding devices due to strain were 2.5, 2.1, 1.5 and 3.1.

【Conclusion】 It was found that thinning GOI by ECR plasma oxidation showed no strain relaxation. The uniform GOI layers with the thickness of 4.5 nm were realized by the present process. As a result, we have successfully fabricated strained ETB GOI pMOSFETs down to the GOI thickness of 4.5 nm by a combination of Ge condensation and plasma oxidation. ETB GOI layer showed on-off current ratio higher than 10^7. The enhancement factors of strained GOI pMOSFETs with 15. 9.2, 6.7 and 4.5 nm-thick GOI against unstrained GOI ones amount to 2.5, 2.1, 1.5 and 3.1, respectively.

【References】[1] S. Nakaharai et al., APL **83**, 3561 (2003) [2] K. Ikeda et al., SSDM, **32** (2008) [3] W.-K. Kim et al., TED 61, 3379 (2014) [4] W.-K. Kim et al., VLSI symp., T9-3 (2017) [5] W.-K. Kim et al., JSAP spring meeting, 21a-S422-7 (2016) [6] Yu et al., IEDM 20 (2015) [7] Hashemi et al., VLSI symp., T16 (2015)

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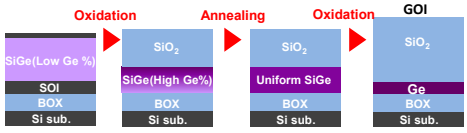

Fig. 1 Process flow of Ge condensation

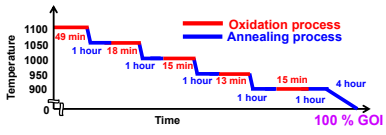

Fig. 2 Ge condensation recipe

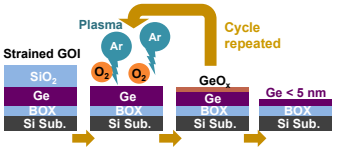

Fig. 3 Process flow of ECR plasma oxidation

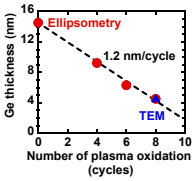

Fig. 4 Ge thickness of GOI layers thinned by digitally etching

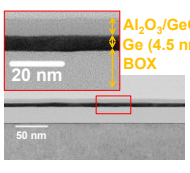

Fig. 6 TEM image of thinned 4.5 nm GOI

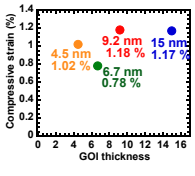

Fig. 5 Compressive Strains in thinned compressively strained GOI layers

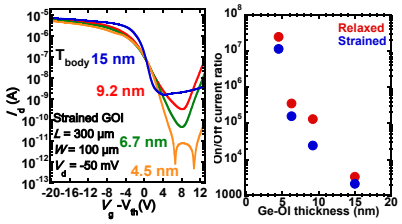

Fig. 7 I_d-V_g curve of strained GOI pMOSFETs

Fig. 8 I_{on}/I_{off} in relaxed and strained GOI pMOSFETs

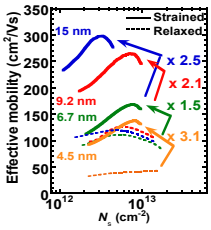

Fig. 9 μ_{eff} of strained and relaxed GOI pMOSFETs