

# Effect of SiGe Layer Thickness in Starting Substrate on Electrical Properties of Ultrathin Body Ge-on-insulator pMOSFET fabricated by Ge Condensation

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**[Background]** Since the on current of conventional Si MOSFETs tends to saturate with scaling, technologies for boosting the carrier transport properties have been attracting a lot of interests. Especially, SiGe or Ge on insulator (SGOI or GOI) pMOSFETs have been regarded as one of the promising technologies to provide high mobility with CMOS compatibility [1]. On the other hand, the Ge condensation method is expected as a promising way to fabricate high quality and ultrathin SGOI/GOI structures [2]. We have recently proposed a new Ge condensation process with the minimized temperature cycles and the slow cooling-down rate [3]. In this study, we investigate the impact of the SiGe thickness of the starting SiGe/SOI substrate on strain in GOI and the performance of GOI pMOSFETs. The remaining strain of the GOI films and the pMOSFET properties are compared between the SiGe thickness of 40 nm and 60 nm in the starting substrates.

**[Experiments]** Fig. 1(a) shows the Ge condensation process. The epitaxially grown Si (10nm)/Si<sub>0.75</sub>Ge<sub>0.25</sub> (40 and 60nm)/SOI (10nm) stacks were prepared as the starting substrate before condensation, as shown in the TEM image of Fig. 1(b). Note that we used SiGe thickness of 60 nm in previous works [3-5]. For comparison, we also applied the condensation recipe with quick and slow cooling-down rates to the substrates with 40 nm-thick SiGe, as shown in Fig. 2. The composition and strain of SGOI/GOI were evaluated by Raman spectroscopy.

**[Results]** Fig. 3(a) and (b) show compressive strain in SGOI as a function of the Ge fraction and the Ge-Ge mode Raman spectra, respectively. Here, the results from 40- and 60-nm-thick SiGe with 4-hour slow cooling, and 40-nm-thick SiGe with the conventional quick cooling are compared. Strain relaxation is effectively suppressed even in a high Ge fraction region (> 0.6) for the slower cooling rate, while the conventional quick cooling produces almost full relaxation for 40-nm-thick SiGe. It is also found that the 40-nm-thick SiGe sample with slow cooling has much higher compressive strain than 60-nm-thick SiGe. This SiGe thickness dependence of strain relaxation can be explained by the difference in the total strain energy. Fig. 4(a) shows the accumulative distributions of compressive strain of the GOI films, evaluated at 2500 points in an area of 100  $\mu\text{m}^2$  in GOI. The thinner SiGe layer is found to have the distribution with the peak shifted toward higher compressive strain. Fig. 4(b) shows the  $I_d$ - $V_g$  curves of GOI pMOSFETs obtained from 40-nm-thick SiGe. The 10-nm-thick ultra-thin-body (UTB) strained GOI pMOSFET obtained from 40-nm-thick SiGe with slow cooling exhibits the higher electrical performance with hole mobility of 342  $\text{V}\cdot\text{cm}^{-1}\cdot\text{s}^{-1}$ .

**[Conclusion]** It is found that higher compressive strain and resulting high hole mobility can be obtained by thinning the Si<sub>0.75</sub>Ge<sub>0.25</sub> layer (40 nm) in the starting substrate of Si/Si<sub>0.75</sub>Ge<sub>0.25</sub>/SOI under the slow cooling down condition after the condensation.

**[References]** [1] S. Takagi et al, Jpn. J. Appl. Phys. **54**, 06FA01 (2015) [2] S. Nakaharai et al., APL **83**, 3561 (2003) [3] W.-K. Kim et al, VLSI Symp., T9-3 (2017) [4] W.-K. Kim et al, IEEE Trans. Electron Devices **61**, 3379 (2014) [5] W.-K. Kim et al, Jpn. J. Appl. Phys. **54**, 04DA05 (2015)

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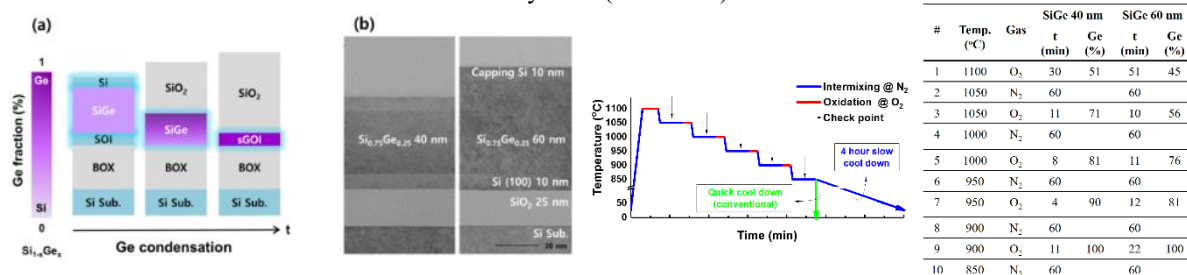


Fig. 1(a) Ge condensation flow (b) TEM image of starting substrate (c) Stepwise condition of condensation recipe

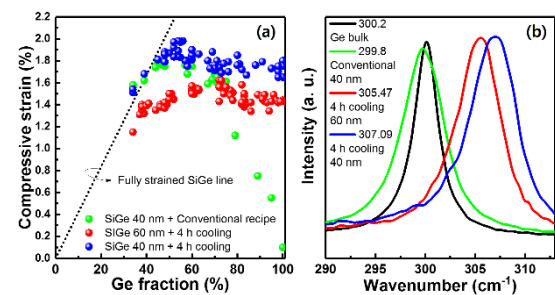


Fig. 3 (a) Compressive strain behavior (b) various Ge peaks of resulting GOI film

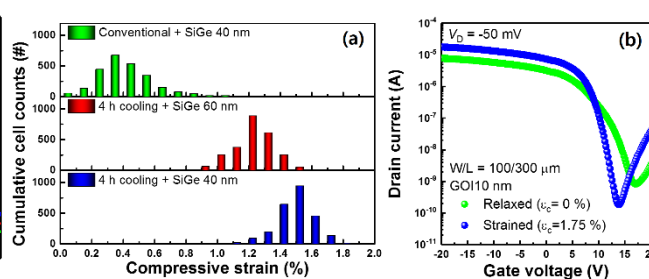


Fig. 4. (a) Distribution of compressive strain (b) Transfer curve of GOI pMOSFET obtained from strained and relaxed GOI film