Effects of gate electrode metal and drain doping concentration on electrical characteristics of Ge/Si hetero-junction tunneling FETs

Tae-Eon Bae, Ryota Suzuki, Ryosho Nakane, Mitsuru Takenaka and Shinichi Takagi
The Univ. of Tokyo
E-mail: taeeon1986@mosfet.t.u-tokyo.ac.jp

1. Introduction A tunneling field-effect transistor (TFET) is one of the most promising concepts for ultra-low power devices, which relies on the band-to-band tunneling mechanism. Development of the optimum materials, structures and process is essential in TFET. As for the TFET sources, pure Ge sources grown on Si are expected to provide higher tunneling current, because of the type-II staggered band alignment between Ge and Si [1]. Thus, this structure can obtain high on/off current ratio and steep subthreshold swing (SS) and some degree of the performance improvement has been demonstrated [2, 3]. Furthermore, in the previous experiments, it has been found that improvement of the TFET performance by forming gas post metallization annealing (PMA) is attributable to reduction in D_{it} [4]. In this study, we have examined the effects of the electrode metal and drain doping concentration on the electrical characteristics of Ge/Si hetero-junction TFETs.

2. Experiment Fig. 1 shows the schematic process flow of the Ge/Si hetero-junction TFETs. A 10-nm-thick silicon-on-insulator (SOI) substrate is used as a starting material. Phosphorus ion implantation (I/I) is used for drain formation. Here, one key process to be optimized is the drain doping concentration. Thus, phosphorus ion dose is varied from 3×10^{14} and 7×10^{14} cm^{-2} to evaluate the effects on the Ge/Si TFET performance. 35-nm-thick in-situ boron-doped Ge layers are grown at 150 °C by molecular beam epitaxy (MBE). 2-step 3.5-nm-thick Al_2O_3 is formed by atomic layer deposition. Subsequently, Al, Ta or W was deposited as the gate metal electrode, followed by Ni and Al deposition for the source contact and the contact pad, respectively. Finally, PMA is carried out in forming gas (4% H_2/N_2) for 30 min at 400 °C.

3. Results and Discussion Fig. 2 shows the I_D-(V_G-V_{TH}) characteristics of the fabricated devices. It is found that the electrical properties of the Ge/Si TFETs such as the on current (I_{on}) and the SS are enhanced in the Al gate metal in comparison with Ta or W. D_{it} at the Al_2O_3/nSi interface is lower in the Al gate metal than that in Ta and W, as shown in Fig. 3, which means that interface properties are affected by gate metal materials. Meanwhile, the drain doping concentration is another critical factor. Fig. 4 shows the I_D-V_G curves as a parameter of the drain I/I dose. I_{off} and SS of the Ge/Si TFETs are improved for the lower I/I dose, attributed to the decrease of the tunneling current in the drain junction. Fig. 5 summarizes SS and gate-induced drain leakage (GIDL) as a function of the drain I/I dose. The values of SS and the GIDL ratio are reduced with lowering the I/I dose. These results mean that the drain doping concentration is also a critical factor for the TFET performance.

4. Conclusion The influence of the gate metal and the drain doping concentrations on the electrical characteristics of Ge/Si hetero-junction TFETs were studied. The higher TFET performance of high I_{on} and steep SS was realized in the Al gate. Also, lower SS and I_{off} were obtained for lower the P I/I dose in the drain regions.

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References [1] O. M. Nayfeh et al., EDL 29 (2008) 1074 [2] M. Kim et al., TED 62 (2015) 9 [3] M. Kim et al., IEEE IEDM Tech. Dig., (2014) pp.331-334 [4] T. Bae et al., JSAP (2017) 16p-412-8

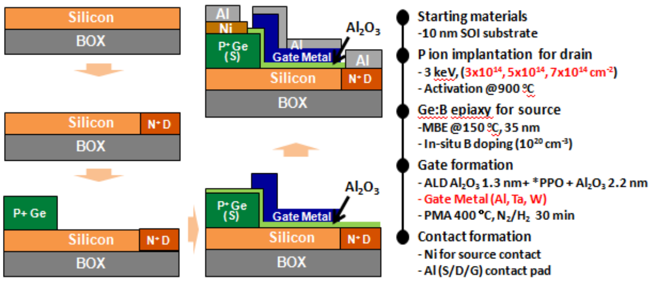

Fig. 1 schematic process flow of the Ge/Si heterojunction TFETs.

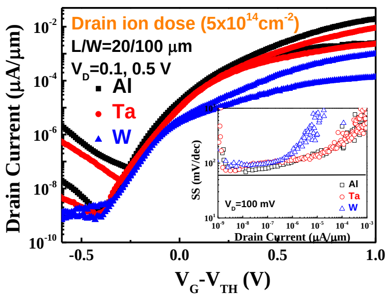

Fig. 2 I_D-V_G characteristics of the fabricated devices.

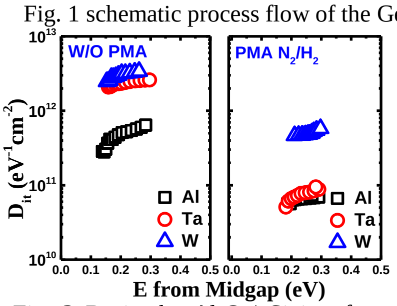

Fig. 3 D_{it} in the Al_2O_3/nSi interface with different gate metal.

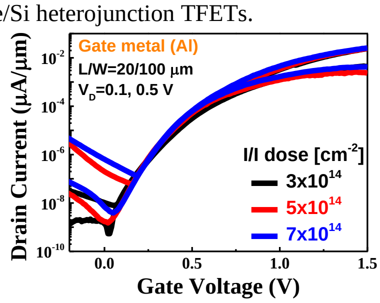

Fig. 4 I_D-V_G curves with different drain ion dose concentration.

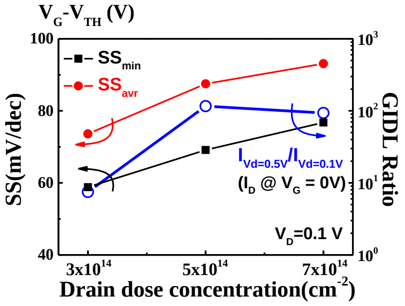

Fig. 5 SS and GIDL ratio with different drain ion dose concentration.