Heavy Ion Generated Current Leading to Long Line-type Soft Errors in Thin BOX SOI SRAMS

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1. Introduction

The silicon-on-insulator (SOI) CMOS technology adopting an thin buried-oxide (BOX) layer has various advantages over conventional structures, including the ability to increase device performance by changing the back-bias [1, 2], as well as higher soft error tolerance [3]. Soft error is defined as a spontaneous error generated by ionizing particles such as ions, neutrons, and protons, when they strike the sensitive region of a device.

Recently, in a heavy ion test, we have discovered a new soft error inside thin-BOX SOI SRAMs, which put its high soft error tolerance in question [4]. It was caused by radiation induced carrier generation under the BOX layer, inside the triple-well structure, which consisted of a repeating pattern of p-well and n-well columns embedded in a deep n-well. A 2 V back-bias was applied to the structure (p-well, n-well, and substrate biased at -2 V, 3.2 V, and 0 V, respectively). Linear energy transfer (LET) up to 70 MeV·cm^2/mg was used in the ion experiment. LET is used to describe the amount of carriers generated along the ion track per track length. Depending on the number of cells flipped by one single ion strike, soft error can be categorized into single bit upset (SBU) and multiple cell upset (MCU). Compared with the case without back-bias, which exhibited mostly SBUs, long MCUs (10 cells or more) along the bit line direction have been observed. The cross-section, which indicates the sensitive region of the device, also increased by more than 100 times. This phenomenon cannot be explained by other previous works [3, 5]. We aim to find the mechanism behind this phenomenon by studying the movement of the ion-generated carriers in the region under the BOX [6].

2. Experimental

HyENEXSS TCAD was used for our study. For simplicity, the region above the BOX as well as the BOX itself was omitted. Only the triple well structure and the substrate were modeled, as shown in Fig. 1. The dimension was obtained by surveys of other works [3, 5], and the bias setting was the same as the ion experiment carried out [4]. At virtual time 1 ns, the ion generates carriers along the ion track, with equivalent LET of 40 MeV·cm^2/mg, which is about 0.4 fC/nm inside Si. This is within the range of typical LET value in a space environment.

3. Result

It is found that the potential of the p-well column that received the ion hit can increase up to 3.3 V, much higher than 1.7 V, an expected value to turn on the nMOS transistor above the BOX. It is also discovered that up to 7 um along the bit line of p-well column suffers a potential increase over 1.7 V. For a typical bit length of 0.5 um, up to 14 cells are expected to flip above the BOX. This result is in agreement with the heavy ion experiment [4].

Fig. 2 shows the current component at 1.001 ns (1 ps after ion strike). An upward current coming from the deep n-well into the p-well contributes to the potential fluctuation of the p-well. This current is caused by the bias difference between deep n-well and p-well and is the main reason behind the long MCUs observed. With this knowledge, optimization of the device to prevent the reported MCUs can be made possible [6].

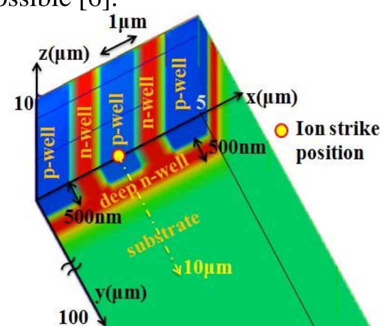

Fig. 1 Simulated triple well structure inside TCAD virtual space.

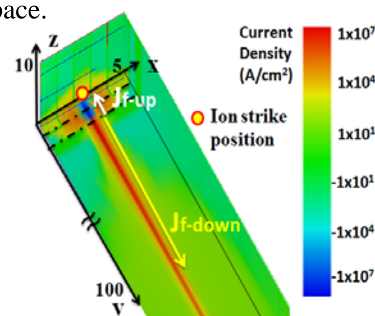

Fig. 2 Vertical (y) components of ion generated current at 1.001 ns.

References

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