Variability Characterictics of Gate-All-Around Polycrystalline Silicon Nanowire Transistors with 10nm-Scale Width

[1]Institute of Industrial Science, The University of Tokyo, [2]Meiji University
°Ki-Hyun Jang[1], Takuya Saraya[1], Masaharu Kobayashi[1], Naomi Sawamoto[2] and Atsushi Ogura[2], and Toshiro Hiramoto[1]
Email: khjang@nano.iis.u-tokyo.ac.jp

[Introduction] Poly-Si nanowire (NW) transistors have attracted attention for 3D multilayer stack integrated circuits and NAND flash memory applications [1]. Most of reported poly-Si NW transistors have width larger than 30nm but few transistors with width of 10nm scale have been reported. In this work, GAA poly-Si NW transistors with 10nm scale width have been fabricated in very controllable manner using electron-beam (EB) lithography. The variability characteristics of threshold voltage (V_{th}) and drain current (I_d) are evaluated [2]. **[Fabrication]** The EB conditions were carefully optimized so that the actual NW width just after RIE (before gate oxidation) is the same as design width (W_d). Fig. 1 shows cross-section TEM images of a fabricated NW transistor. The trapezoid-shaped GAA structure is confirmed. The width of top and bottom are ~5nm and 15nm, respectively. **[Results]** Fig. 2 shows I-V characteristics of a planar transistor and the NW transistor (W_d=15nm, L=300nm, the specific transistor whose cross-section is shown in Fig. 1). In the NW transistor, electrical properties are improved because the total number of grain boundaries and traps are reduced by scaling poly-Si film. Fig. 3 shows variability characteristics. To make a fair comparison with reported data [3], the Pelgrom plot is shown in Fig. 4. $\sigma V_{th}/T_{inv}$ is evaluated to cancel the effect of T_{inv} for V_{th} variability [3] and overdrive voltage (V_g–V_{th}) is fixed for I_d variability [3]. Smaller or comparable variability than that of reported poly-Si NW transistors [3] is confirmed. **[Summary]** GAA Poly-Si NW transistors with width of 10 nm scale were fabricated under precise width control and small variability is confirmed. **[References]** [1] J. K. Park et al., VLSI, p. 1 (2014). [2] K. H. Jang et al., SNW, p. 33 (2017). [3] M. Saitoh et al., VLSI, p. 222 (2014).

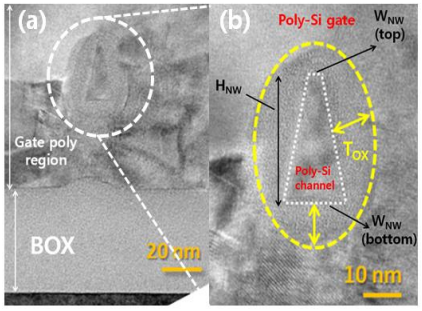

Fig. 1. (a) A cross-sectional TEM image of fabricated GAA structure. (b) An enlarged image.

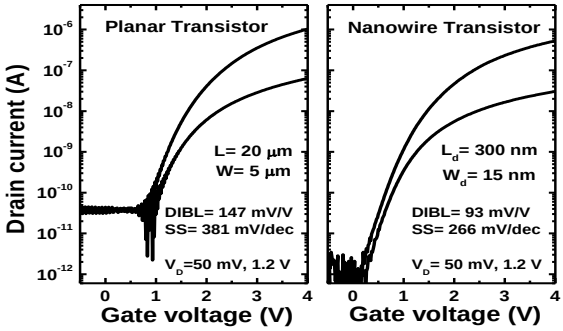

Fig. 2. I-V characteristics of a planar transistor and a nanowire transistor.

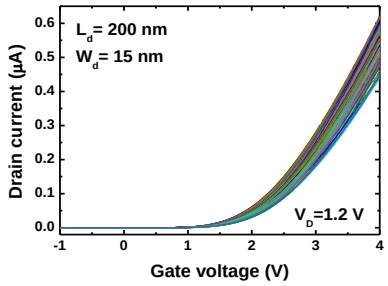

Fig. 3. I_d-V_g characteristics of 90 nanowire transistors.

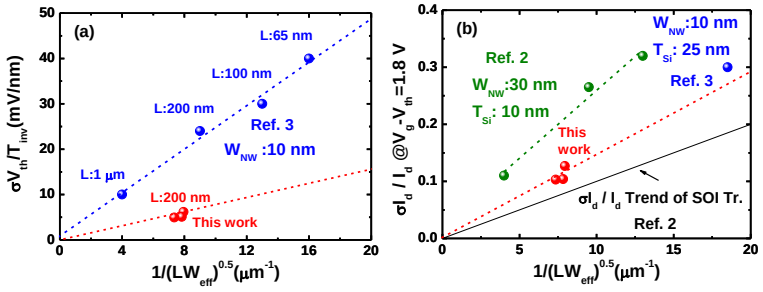

Fig. 4. Pelgrom plots of (a) $\sigma V_{th}/T_{inv}$ and (b) $\sigma I_d/I_d$ at V_{ds}=1.2V. L is 200nm and W_d is varied from 14nm to 20nm. The perimeter of GAA is used as W_{eff}.