冷却レートを低減した酸化濃縮プロセスにより作製した高圧縮ひずみ GOI pMOSFET

High compressive strain GOI pMOSFET fabricated by Ge condensation process with reduced cooling rate

°金佑彊，竹中充，高木信一
東大院工
°Wu-Kang Kim, Mitsuru Takenaka and Shinichi Takagi
The University of Tokyo
Email: wukangkim@mosfet.t.u-tokyo.ac.jp

【Background】With fundamental limits of scaling Si MOSFETs, Ge is expected to be one of the most promising next generation channel materials because of both high electron and hole mobility and easy introduction into the Si platform. Moreover, the UTB (Ultra-thin body) GOI (Ge-on-Insulator) structure is very important to suppress the short channel effect. Among the several GOI fabrication methods, the Ge condensation method [1, 2] is one of the most promising techniques to fabricate UTB GOIs. However, one of the most serious problems in Ge condensation has been the strain relaxation during the condensation process [3], which not only causes defects in GOI layers but also prevents mobility enhancement in pMOSFETS. Even though we have recently reported a new Ge condensation process which enabled to suppress strain relaxation during the process[4], the impact of the cooling time on remaining strain and the resulting pMOSFET mobility has not been examined yet. In this paper, we examine the effect of the cooling time in Ge condensation on strain and performance of fabricated GOI pMOSFET with compressive strain.

【Experimental】Fig. 1 shows the process flow of UTB GOI layers with the Ge condensation process, where the oxidation temperature is changed from 1100 °C, to 1050 °C, 1000 °C, 950 °C and 900 °C. After each oxidation step, intermixing annealing was performed in N_2 at 1050 °C, 1000 °C and 950 °C, according to [5]. In the conventional Ge condensation, SiGe-OI wafers were taken out from an oxidation furnace after each oxidation step to check the Ge composition. On the other hand, the new Ge condensation process [4, 6] employs the oxidation/annealing in the furnace without taking out the wafers during the process (Fig. 2 (a), (b)). GOI wafers were cooled down in 3 different ways after the new Ge condensation (Fig. 2 (c)), in order to examine the impact of the cooling rate on the strain relaxation. The 3 different cooling rates, 4-hour slow cooling, natural cooling (~2.5 hours) and the conventional rapid cooling(< 1 min) were used. The spatial disbribution of strain over GOI layers was evaluated from the Ge peak shift in Raman spectroscopy. Also, backgate operation GOI pMOSFETs with Ni S/D with Al backgate were fabricated for each strained GOI with different cooling rates.

【Results】Fig. 3 shows the cumulative distribution of strain in the GOI layers. The mean strain values in GOI layers after 4-hour linear cooling, natural cooling, and rapid cooling are estimated as 1.17, 1.06, and 0.79%, respectively, with the standard deviation of 0.23, 0.26, and 0.29. These values indicate that slower cooling can lead to higher compressive strain and the tighter strain distribution. As a result, we can conclude that rapid decrease in temperature can cause strain relaxation, presumably due to the difference in the thermal expansion coefficient between Ge and SiO_2/Si. Fig. 4 shows the I_d-V_g characteristics of GOI pMOSFETs. The enhancement in I_{on} was observed due to strain effect. As shown in Fig. 5, the effective hole mobility of pMOSFETs by the conventional process (relaxed), new condensation process with natural cooling (1.06 % strain) and 4 hour cooling (1.17 % strain) amount to 120, 242 and 301 cm^2/Vs, respectively.

【Conclusion】We have examined how the cooling affect strain in the Ge condensation process. The slower GOI cooling process with the continuous oxidation/annealing in furnace resulted in higher compressive strain in GOI layers, which enhanced hole mobility in pMOSFETs with ehnacement factor of 2.5.

【Acknowledgment】This work was partly supported by JST-CREST Grant Number JPMJCR1332, Japan and a Grant-in-Aid for Scientific Research on Priority Area (No. 26249038) from MEXT.

【References】[1] S. Nakaharai *et al.*, APL **83**, 3561 (2003) [2] K. Ikeda *et al.*, SSDM, 32 (2008) [3] T. Tezuka *et al.*, APL, 90 (2007) [4] W.-K. Kim et al., JSAP spring meeting, 21a-S422-7 (2016) [5] W.-K. Kim et al., TED **61**, 3379 (2014) [6] W.-K. Kim et al., VLSI symp., T9-3 (2017)

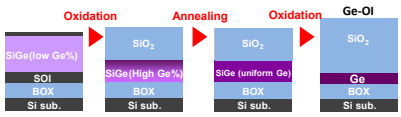

Fig. 1 Process flow of Ge condensation.

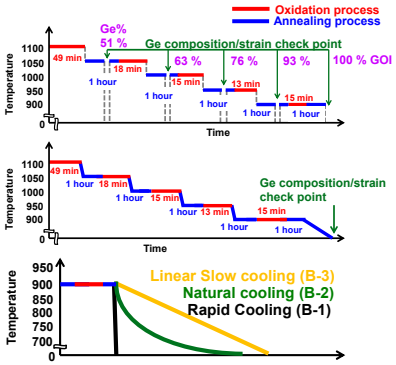

Fig. 2 Conventional (above) and new Ge condensation (middle) recipes with 3 different cooling down methods (below)

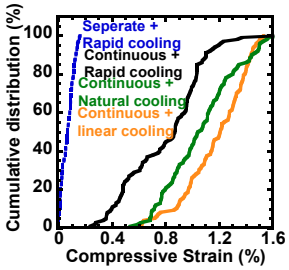

Fig. 3 Strain behavior of different

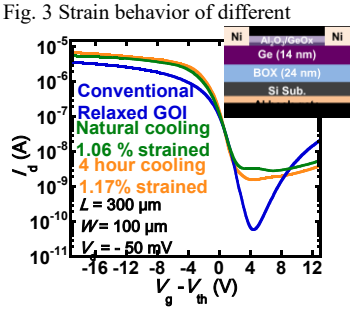

Fig. 4 I_d-V_g characteristics of GOI pMOSFETs

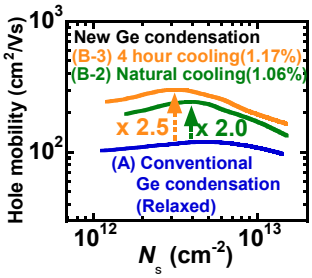

Fig. 5 μ_{eff} of GOI pMOSFETs