常温で表面活性化接合した Si/GaAs 界面の原子・電子構造

Atomistic structure of Si/GaAs interfaces fabricated by surface-activated bonding at RT

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【Introduction】 A surface-activated bonding (SAB) method at room temperature, in which surfaces of substrates are activated by Ar atom-beams prior to bonding, is recently applied to form Si/GaAs interfaces with a low interface resistance,[1] and InGaP/GaAs/Si hybrid triple-junction cells with a conversion efficiency above 26% are fabricated.[2] The interface resistance varies depending on the SAB condition of Ar atom irradiation and post-growth annealing,[1] even though the origin of the resistance is unclear. Accordingly, a comprehensive knowledge of the electrical property at the interfaces depending on their atomistic structure is indispensable to fabricate high-efficiency cells by optimizing the interface structure.

【Experiments】 Si/GaAs interfaces were fabricated under a SAB condition at room temperature,[1] with the substrates of B-doped (001) p-Si (with a carrier concentration of 2×10^{14} cm^{-3}) and Si-doped n-GaAs (2×10^{16} cm^{-3}) which was 5° off from (001) towards [110]. Parts of the SAB interfaces were then annealed at 473 K or 673 K for 1 minute. The Si surface and the GaAs one in the SAB interfaces were determined separately by plane-view TEM with the reflection of **g** = [220] for GaAs and that for Si, respectively.

【Results & discussions】 In an as-bonded SAB interface, there was a partially-amorphized Si (a-Si) layer (~3nm thick) on the Si substrate, introduced during the surface activation process, and a thin Si oxide layer (less than ~0.5nm thick) existing at the GaAs/a-Si interface, introduced during the post-activation processes. While the Si/a-Si interface was smooth, the GaAs/a-Si interface was strained presumably due to dimples (~5nm in size) on the GaAs substrate introduced by Ar atoms, dumps (~20nm in size) at dislocations passing through the GaAs surface, and Si oxides on the Si substrate. Those strains were reduced by annealing according to the recrystallization of the a-Si layer, and this would result in the reduction of the interface resistance.[1] It is therefore hypothesized that the interface resistance would be originated from the defects at the GaAs/a-Si interface, and the resistance might be reduced further by smoothing a surface on the GaAs substrate and by removing the Si oxides on the a-Si layer, via optimization of the SAB condition.

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