Breakdown Voltage Instability in nLDMOS Transistors

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High-voltage lateral diffused metal-oxide-semiconductor (LDMOS) transistors are widely used in applications such as power management and LCD driver. Because LDMOS devices are operated under high voltages, the drain breakdown voltage ($V_{bd}$) is a key device parameter. $V_{bd}$ increase has been observed after either repeated $V_{bd}$ measurements [1] or hot-carrier stress [2], leading to $V_{bd}$ instability. There is few experimental verification concerning the root cause of $V_{bd}$ increase. In this work, we investigate the mechanism of hot-carrier induced $V_{bd}$ increase in nLDMOS transistors by charge pumping measurements [3] and TCAD simulations.

Fig. 1 shows the structure of the n-type LDMOS transistor, which is fabricated with a CMOS compatible process, used in this work. The channel (ch), n accumulation (acc), and n drift regions below STI (bs) is also drawn in Fig. 1. $V_{bd}$ is the drain voltage ($V_d$) when the drain current ($I_d$) reaches 1 nA with the source, gate, and bulk terminals grounded. To study hot-carrier induced $V_{bd}$ instability, device was stressed at $V_d = 1.1V_{dd}$, where $V_{dd}$ is operating voltage. The gate voltage ($V_g$) at stress is the $V_g$ that produces the peak bulk current. The stress test was lasted for 3000 s and measured the shift of device parameters and charge pumping current ($I_{CP}$) periodically. In $I_{CP}$ measurement, a pulse of 3 V in height at 500 kHz was applied to the gate with the base voltage ($V_{base}$) sweeping from -4 to 0 V.

Fig. 2 shows hot-carrier induced $V_{bd}$ increase, where $V_{bd}$ of fresh device is 47 V but it increases to 57 V after 3000 s stress even though the stress induced linear-region $I_d$ ($I_{lin}$) is degraded only 2.4% as in inset. To investigate the mechanism of this $V_{bd}$ increase, $I_{CP}$ of the fresh and aged device during stress were measured as in inset of Fig. 3. From $I_{CP}$ data, hot-carrier induced interface stages ($\Delta N_{IT}$) in channel and accumulation regions can be extracted by $\Delta N_{IT} = \Delta I_{CP} / (qFWL_{CP})$, where $\Delta I_{CP}$ and $L_{CP}$ are the increase in $I_{CP}$, and the length of region where $N_{IT}$ is probed [3]. The extracted $\Delta N_{IT}$ is shown in Fig. 3, where $\Delta N_{IT}$ in the accumulation region is much greater than the $\Delta N_{IT}$ in the channel region. This suggests that $\Delta N_{IT}$ in accumulation region is very likely the root cause of $V_{bd}$ increase.

To verify the impact of $\Delta N_{IT}$ location on $V_{bd}$, TCAD simulations of $V_{bd}$ were performed for the following cases: a device without $\Delta N_{IT}$, a device with a fixed amount of $\Delta N_{IT}$ in the channel region, accumulation region, and drift region below STI. Fig. 4 shows that device without $\Delta N_{IT}$, device with $\Delta N_{IT}$ in the channel region or drift region below STI all has $V_{bd} \sim 47$ V. The device with $\Delta N_{IT}$ in accumulation region has $V_{bd} \sim 58$ V. The inset of Fig. 4 compares the impact ionization generation for a device without $\Delta N_{IT}$ and a device with $\Delta N_{IT}$ assigned in the accumulation region at $V_d = 47$ V. $\Delta N_{IT}$ in accumulation region significantly reduces the impact ionization generation as seen in inset (b) of Fig. 4, leading to $V_{bd}$ increase. From the above analyses, it is verified that hot-carrier induced $N_{IT}$ generated in the accumulation region is responsible for $V_{bd}$ instability in our nLDMOS transistors.

Fig. 4 $V_{bd}$ of $\Delta N_{IT}$ in different locations. Inset is impact ionization without/with $\Delta N_{IT}$ in acc region.