Enhancement-Mode Ga_2O_3 MOSFETs with Si-Ion-Implanted Source and Drain

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Power converters favor normally-off switches for safety and simplified circuit topologies. Enhancement-mode Ga_2O_3 metal-oxide-semiconductor field-effect transistors (MOSFETs) reported to date employ relatively high channel doping intended for maintaining volume current density, which imposes constraints on the device dimensions or architecture to realize positive threshold voltage (V_T) while limiting conductance in the ungated access regions [1,2]. This work demonstrates enhancement-mode Ga_2O_3 MOSFETs with an unintentionally-doped (UID) Ga_2O_3 channel, whose low background carrier density (n_{UID}) offers improved design flexibility and reduced process complexity for achieving full channel depletion at a gate bias (V_{GS}) of 0 V. Low source/drain series resistances were realized by Si-ion (Si^+) implantation. MOSFETs with a channel length of 4 µm delivered a maximum drain current density (I_{DS}) of 1.4 mA/mm and an I_{DS} on/off ratio (I_{ON}/I_{OFF}) near 10^6.

The enhancement-mode Ga_2O_3 MOSFETs consisted of a 1.2-µm-thick UID Ga_2O_3 epilayer grown on an Fe-doped semi-insulating β-Ga_2O_3 (010) substrate by ozone molecular beam epitaxy (Fig. 1). Si^+ implantation defined the n^+ source/drain ohmic and access regions. A 50-nm-thick Al_2O_3 gate dielectric was formed on the Ga_2O_3 by plasma atomic layer deposition. A gate-n^+ overlap of 5 µm at both the source and drain sides led to highly conductive access regions and ensured charge modulation over the entire 4-µm-long channel. MOS capacitors (MOSCAPs) with a 200-µm-diameter circular anode were used for capacitance-voltage (*C-V*) characterization of the Al_2O_3 dielectric. Vertical Pt/Ga_2O_3 Schottky barrier diodes (SBDs) with a 2-µm-thick UID Ga_2O_3 drift layer were fabricated on a Sn-doped n^+ β-Ga_2O_3 (010) substrate for extracting n_{UID}.

C-V measurements performed on the SBDs indicated that the UID Ga_2O_3 drift layer was fully depleted by the built-in voltage, based on which the n_{UID} was estimated to be less than 4×10^{14} cm^{-3}. The MOSFETs featured small parasitic source/drain resistances, where a sheet resistance of 84 Ω/sq for the n^+ implant and a metal/semiconductor contact resistance of 0.25 Ω·mm yielded a total parasitic resistance of 1.4 Ω·mm between source and drain. Despite a low n_{UID}, the maximum on-state I_{DS} of 1.4 mA/mm was an order of magnitude higher than those reported in Refs. 1 and 2 (Fig. 2). An $I_{ON}(V_{GS}$=+38 V$)/I_{OFF}(V_{GS}$=0 V$)$ ratio of 9×10^5 was achieved at V_{DS}=15 V (Fig. 3). Improved device characteristics can be expected by optimizing the Al_2O_3 dielectric to eliminate hysteresis, Fermi level pinning, and large V_T shift that were attributable to a high density of electron traps as revealed by the MOSCAPs.

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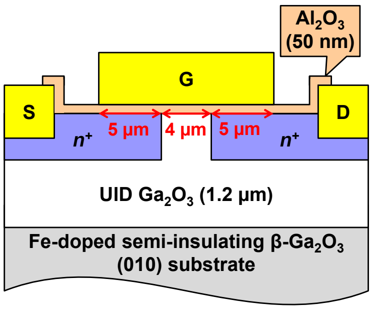

Fig. 1. Schematic cross section of the enhancement-mode Ga_2O_3 MOSFET.

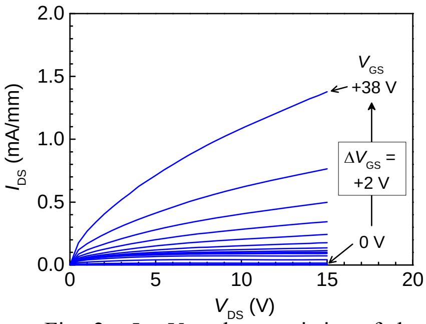

Fig. 2. I_{DS}-V_{DS} characteristics of the enhancement-mode Ga_2O_3 MOSFET.

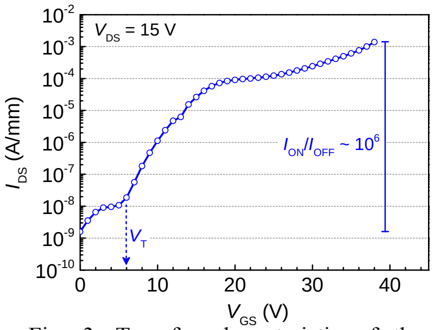

Fig. 3. Transfer characteristic of the same MOSFET as extracted from Fig. 2.