## Mg Ion Implantation Technology for Vertical Ga<sub>2</sub>O<sub>3</sub> Power Devices

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Vertical *n*-Ga<sub>2</sub>O<sub>3</sub> power devices make use of insulating or *p*-type materials for forming current blocking layers (CBLs) to prevent direct source-drain leakage. Mg-ion (Mg<sup>++</sup>) implanted Ga<sub>2</sub>O<sub>3</sub> was investigated in this work as a CBL in light of semi-insulating Ga<sub>2</sub>O<sub>3</sub> obtained by Mg compensation doping of *n*-type bulk crystals. Systematic thermal anneals and electrical measurements presented evidence of implant activation and illustrated a pathway for forming CBLs in Ga<sub>2</sub>O<sub>3</sub> devices.

Test structures comprising *n*-Ga<sub>2</sub>O<sub>3</sub>/Ga<sub>2</sub>O<sub>3</sub>:Mg(CBL)/*n*-Ga<sub>2</sub>O<sub>3</sub> were fabricated on Si-doped  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> (001) epilayers (5–7 µm, *n*~10<sup>16</sup> cm<sup>-3</sup>) grown by halide vapor phase epitaxy on Sn-doped (*n*~3×10<sup>18</sup> cm<sup>-3</sup>) substrates. Mg<sup>++</sup> implantation was performed at 560 keV and a dose of 4×10<sup>13</sup> cm<sup>-2</sup> with a peak concentration of 1×10<sup>18</sup> cm<sup>-3</sup> at ~0.6 µm below the surface. Capless thermal anneals were carried out at 800, 900, and 1000°C for 30 min in N<sub>2</sub> to attempt Mg activation and implantation damage recovery. A 100-nm-thick *n*<sup>+</sup> top contact layer was formed by Si ion implantation. Patterned-top and blanket-bottom Ti/Au ohmic electrodes were subsequently deposited for current-voltage measurements to assess vertical conduction through the Mg<sup>++</sup>-implanted Ga<sub>2</sub>O<sub>3</sub> (Fig. 1). Pt Schottky electrodes were also deposited for capacitance-voltage (*C-V*) analysis.

Ga<sub>2</sub>O<sub>3</sub> as-implanted with Mg<sup>++</sup> was highly resistive owing to lattice damage. Leakage through the CBL annealed at 800°C remained low (<1 mA/cm<sup>2</sup> at 200 V) as only limited damage reversal had taken place. A higher annealing temperature of 900°C led to significantly increased conduction through the CBL (1 mA/cm<sup>2</sup> at 60–90 V) consistent with improved crystal quality. However, the effect of damage recovery saturated beyond 900°C and only slight degradation in current blocking capability (1 mA/cm<sup>2</sup> at 40–80 V) was observed with 1000°C annealing. The similar blocking characteristics between structures annealed at 900°C and 1000°C suggested that the electron barrier was no longer dominated by lattice defects; instead, a distinct mechanism that could be unambiguously ascribed to Mg activation as compensating acceptors had given rise to a new barrier in the current path. In addition, Mg diffusion observed in all annealed samples led to uniform Mg depth profiles at a level consistent with the background Si doping (Fig. 2), resulting in carrier compensation throughout the epilayers as revealed by *C-V* measurements (Fig. 3). CBLs with well-defined thicknesses and doping can thus be conceived by controlling the implant dosage and annealing conditions.

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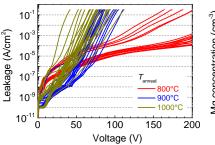


Fig. 1. Vertical leakage through annealed  $Mg^{++}$ -implanted  $Ga_2O_3$ .

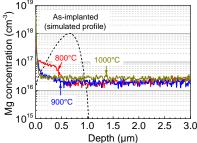


Fig. 2. Secondary ion mass spectroscopy depth profiles of Mg showing significant diffusion upon thermal annealing.

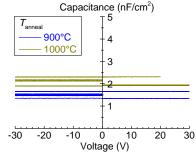


Fig. 3. Flat *C-V* profiles of fullycompensated epilayers annealed at 900 and 1000°C as a result of Mg diffusion and activation as acceptors.