1. Introduction

For future ultimately scaled CMOS devices, ultra-thin-body (UTB) germanium-on-insulator (GeOI) technology is a promising platform to realize Ge CMOS devices with stronger gate control and immunity against short channel effects. However, severe mobility degradation has been reported in the commercially available Smart-Cut™ GeOI substrates with body thickness ($T_{\text{body}}$) less than 10 nm. Therefore, more sophisticated fabrication methods of UTB-GeOI substrates are strongly required for improving UTB-GeOI device performance.

2. Experimental procedures

UTB-GeOI substrates with and without Si-passivated back interface (SBI) were prepared through Hetero-Layer-Lift-Off (HELLO) technique.[2,3] After Ge active regions mesa isolation, an Al$_2$O$_3$ gate insulator was deposited at 200 °C in a plasma-enhanced ALD chamber. The TaN metal gate was then fabricated through sputtering and RIE. Subsequently, a thin Ni layer was deposited onto the S/D regions by an e-beam evaporator after Al$_2$O$_3$ gate insulator wet etching. NiGe metal S/D was then formed by rapid thermal annealing and the unreacted Ni was removed by HCl solution.

3. Results and discussions

Fig. 1 shows the $T_{\text{body}}$ dependence of the effective hole mobility for UTB-GeOI $p$-MOSFETs with and without SBI. The highest peak hole mobility in this work is around 240 cm$^2$/Vs in the UTB-GeOI $p$-MOSFETs with SBI. The insertion of an ultra-thin Si layer helps to maintain the mobility at a wide range of sheet carrier density ($N_s$) and obvious degradation owing to thinner GeOI is not observable. This can be attributed to the reduction of interfacial trap density between Ge and BOX, thus suppressing the Coulomb scattering in UTB-GeOI channel.[4] Besides, SBI, which works as an energy barrier layer for holes, provides conformal hole confinement at Ge/Si interface, suppressing the effect of GeOI thickness fluctuation on mobility. Under the same $T_{\text{body}}$ of 4 nm, the effective hole mobility of UTB-GeOI $p$-MOSFETs with SBI at $N_s$ of 5×10$^{12}$ cm$^{-2}$ increases by about five times as compared with devices without SBI, revealing Si passivation is promising in enhancing the hole mobility even in the UTB regime less than 10 nm.

4. Conclusion

UTB-GeOI $p$-MOSFETs with body thickness of only 4 nm and Si-passivated back interface have been successfully fabricated by HELLO technique. The insertion of ultrathin Si layer helps to suppress the Coulomb scattering from the back interface and enhance the mobility of UTB-GeOI $p$-MOSFETs.

References