Diamond NOT and NOR logic circuits

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It is well-known that wide bandgap semiconductors such as GaN, SiC, and diamond are suitable to replace silicon partly for fabrication of high-power and high-frequency electronic devices because of their large band-gap energies, high carrier mobility, and high breakdown field. According to figure of merit, diamond-based electronic devices have the largest power-frequency product, the highest thermal limitation, and the lowest power-loss at high-frequency. Thus, diamond semiconductor devices are expected to be of very importance for the future practice applications. Recently, controlling conditions for depletion-mode (D-mode) and enhancement-mode (E-mode) hydrogenated diamond (H-diamond) metal-oxide-semiconductor field-effect transistors (MOSFETs) have been clarified [1]. There are two necessary conditions for fabrication of E-mode H-diamond MOSFETs, which are a bilayer gate oxide structure deposited by atomic layer deposition (ALD) and sputtering deposition (SD) techniques, and annealing at 150-350 °C for the devices. The ALD-oxide with a thickness of 4.0 nm impacts as a buffer layer for the deposition of SD-oxide. On the other hand, even there is an annealing process for the H-diamond MOSFET with a single ALD-Al_2O_3 layer as the gate oxide, the MOSFET still operates with a D-mode characteristic. After improving the electrical properties of H-diamond MOSFETs and fabricating D/E-mode H-diamond MOSFETs controllably, next challenge is to combine these devices to be logic circuits. In this study, the H-diamond NOT and NOR logic gates composed of D-mode ALD-Al_2O_3/H-diamond and E-mode SD-$LaAlO_3$/ALD-Al_2O_3/H-diamond MOSFETs will be fabricated.

Fig. 1 (a) shows voltage transfer characteristics (VTCs) of the H-diamond E/D-mode NOT logic gate with the V_{DD} changing from −5.0 to −25.0 V. There are distinct inversion characteristics for the input signal of the H-diamond E/D-mode MOSFET NOT gate. If the V_{in} is 0 V, the E-mode $LaAlO_3$/Al_2O_3/H-diamond MOSFET is in the off-stage, resulting in V_{out} close to V_{DD}. Likewise, if the V_{in} is −10.0 V, the E-mode $LaAlO_3$/Al_2O_3/H-diamond MOSFET turns on, resulting in V_{out} close to the ground level. Gain curve defined by $-dV_{out}/dV_{in}$ in the VTCs can be deduced and shown in the Fig. 1 (b). The maximum gain value increases from 1.1 to 26.1 with the V_{DD} changing from −5.0 to −25.0 V. Fig. 1 (c) shows the V_{out} of the H-diamond D/E-mode MOSFET NOR gate as functions of V_{in}. There are four states for the input voltages of logical (1, 1), logical (1, 0), logical (0, 1), and logical (0, 0). For each V_{in} state, the measurement time is 60 s. If both V_{in1} and V_{in2} are −10.0 V [logical (1, 1) state], the V_{out} is −0.85 ±0.05 V and logical 0. If the V_{in1} and V_{in2} are −10.0 and 0 V, respectively [logical (1, 0) state], the V_{out} is −1.86 ±0.10 V and logical 0. If the V_{in1} and V_{in2} are 0 and −10.0 V, respectively [logical (0, 1) state], the V_{out} is −1.92 ±0.10 V and logical 0. If both V_{in1} and V_{in2} are 0 V [logical (0, 0) state], the V_{out} is −10.0 V and logical 1. These results indicate that our logic gate operates with the NOR characteristics.

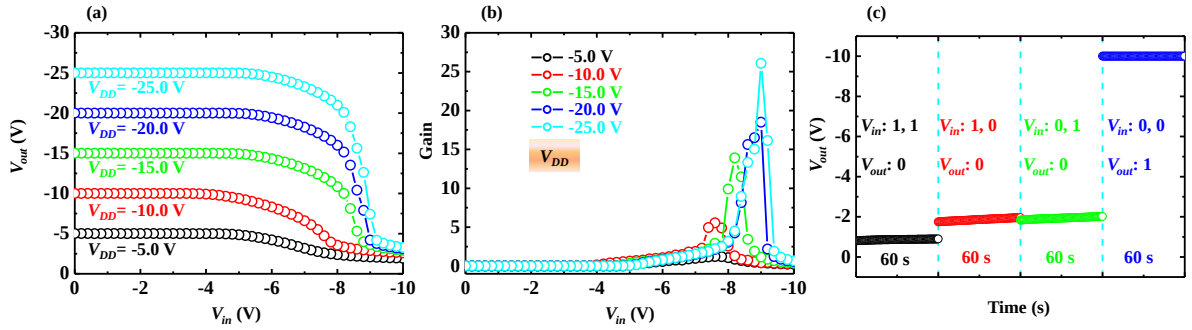

Fig.1 (a) VTCs of the H-diamond D/E-mode MOSFET NOT gate with the V_{DD} changing from −5.0 to −25.0 V, (b) the gain curve ($-dV_{out}/V_{in}$) derived from the VTCs, and (c)V_{out} of the H-diamond D/E-mode MOSFET NOR gate as functions of four V_{in} states. The measurement time for each state is 60 s.

Reference

[1] J. W. Liu, M. Y. Liao, M. Imura, T. Matsumoto, N. Shibata, Y. Ikuhara, and Y. Koide, J. Appl. Phys. **118**, 115704 (2015).