表面を改質した Ge 表面における Schottky 特性

Schottky diode characteristics at metal/surface-damaged Ge

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Fermi-level pinning of metal/Ge interface

The Fermi-level pinning (FLP) at metal/Ge interface is very strong [1], and the metal work function has nothing to do with the Schottky barrier height (SBH) observed experimentally. This is a big challenge in Ge n-channel MOSFET technology, because the pinning level is located near the valence band edge of Ge and the contact resistance at metal/n^+Ge should be intrinsically high. The FLP mechanism has been experimentally and theoretically investigated for a long time. It is, however, still a big issue. A big debate is whether it is intrinsic (MIGS) or extrinsic (DIGS). In any cases, FLP should be affected by both metal and semiconductor sides. In this work, we have paid attention to the semiconductor side, particularly to Schottky diode characteristics at intentionally damaged Ge surface.

Effect of Ge surface damages on Fermi-level pinning

SBH for n-substrate is generally described by $\Phi_{bn} = S(\Phi_M - \chi) + (1 - S)\Phi_{CNL}$, in which S and Φ_{CNL} are the pinning parameter and charge-neutrality level (CNL). Ge surface modification should affect both S and Φ_{CNL}. In addition, χ might also be affected. In the present experiment, Ge surface was modified by Ge ion implantation (acceleration voltage of 100 kV and dose of 1 x10^{14}/cm^2), followed by annealing at various temperatures. **Fig. 1** shows I-V characteristics of Al/implanted-Ge annealed at various temperatures in N_2. With an increase of annealing temperature, the reverse leakage current is lowered. This fact means the Schottky diode characteristics are surely affected by the surface quality of Ge.

A couple of points should be noticed. (i) Implanted Ge surface including cases with implanted dopants (P, As, Sb or B) may be different from the initial single crystalline Ge surface even after 625°C anneal. The contact resistance at metal/Ge may not be simply described by the conventional formula [2]. (ii) The remaining defects may change the CNL at the surface. The ohmic characteristic is, however, not observed even in the relatively higher annealing temperature case. It means that the ohmic behavior obtained experimentally [3, 4] is not due to the defect annihilation but due to an intrinsic Fermi-level pinning alleviation. (iii) Advanced methods such as double implantation / laser annealing to enhance the dopant activation should be carefully discussed from the viewpoint of remaining defects and/or imperfect crystallinity. (iv) It should be careful in case of metal deposited by sputtering or ion-beam processes on Ge, because the surface damages on Ge are not easily annihilated.

This view is also supported by the imperfect recovery of the peak FWHM in Raman measurement of Ge-implanted surface (**Fig. 2**) [5].

Conclusion

Ge-implanted Ge surface shows high reverse leakage current even after thermal annealing. This fact suggests that the FLP on the ion-damaged Ge surface should be carefully considered from extrinsic viewpoints of defect-mediated conduction rather than the change of S or Φ_{CNL}.

Ref. [1] T. Nishimura, et al., APL **91**, 123123 (2007), [2] S. Z. Sze, Physic of Semiconductor Devices 3rd ed., (Wiley 2007). [3] T. Nishimura, et al., APEX **1**, 051406. [4] T. Nishimura, et al., APEX **9**, 081201. [5] 中村俊充他，2014 年春季応物学会.

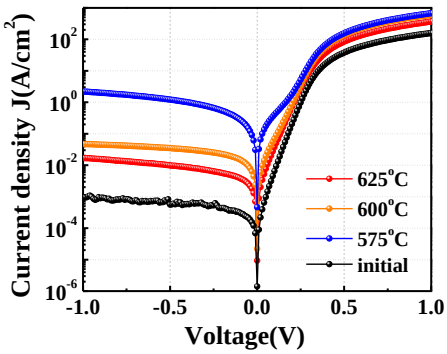

Fig. 1　Room temperature I-V characteristics of Al/Ge damaged by Ge implantation, followed by annealing at various temperature in N_2 for 5 min. (electrode diameter 100 μm^{ϕ})

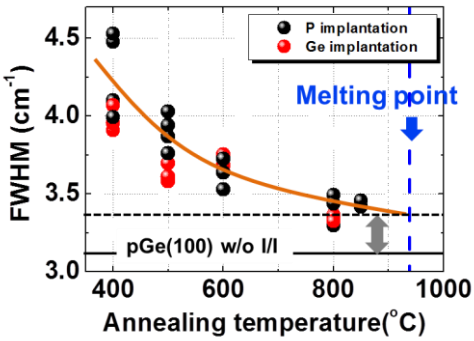

Fig. 2　FWHM of Raman spectroscopy of P or Ge implanted Ge as a function of annealing temperature [5]. Even after 800°C anneal, the FWHM is not recovered to the initial.