Multi-bit Memory Effect in an Organic Field Effect Transistor using a Charge Storage Polymer

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Memory effect in an organic field effect transistor (OFET) could be achieved by using a thin film of polymer as charge storage layer.[1–3] The trapped charges at the trapping layer cause the change in drain current (I_D) or the shift of threshold voltage (V_{th}) of the OFET, which corresponds to the different states of the memory. An 1-bit devices could be fabricated by using a polymer layer of Cytop,[1] poly methylmethacryrate (PMMA) [2] or poly(α-methylstyrene) (PαMS).[3] However, for a multi-bit application, the OFET must exhibit several distinguished logic states and each state could be easily controlled by a programmed voltage applied to the gate. In this paper, a multi-bit OFET memory using a charge storage polymer of poly(vinyl cinammate) (PVCN) is reported.

A substrate of silicon wafer with 400 nm-thick of silicon dioxide (SiO_2) was used after cleaning. Subsequently, a 10 nm-thick of PVCN was fabricated by spin coating onto the SiO_2 surface using a solution of PCVN in monochrolobenzene (2.5 mg/ml) followed by UV exposure for photochemical crosslink and baking at 140°C for 1 h. Finally, an active layer of pentacene (50 nm) and copper source/drain (S/D) electrodes (50 nm) were thermally deposited.

The fabricated memory OFET exhibited a p-type characteristics with a mobilitiy (μ) of 0.29 $cm^2V^{-1}s^{-1}$, a V_{th} of -11.54 V and an on/off ratio of 2.53×10^5, which are similar to those in other reports.[1,4] FiguresP 1 and 2 show the shifts of V_{th} under negative voltages applied to the gate for 3 sec, sweeping from -100 V to -200 V. At programming voltages below -100 V, the V_{th} does not shift much. On contrary, at higher programming voltages of -160 V, -180 V and -200 V, three ΔV_{th} of approximate 9.4 V, 18.3 V, and 27.8 V were observed.(Fig. 2) The initial state and the programming states by applying voltages of -160 V, -180 V and -200 V to the gate correspond to 4 logic states of a multi-bit memory. After programming, the memory was attempted to erase by applying a positive voltage to the gate. Although a voltage of 200 V was applied, only a negligible shift of V_{th} has been observed. This indicates that the memory OFET exhibits the write-once-read-many memory characteristics. The stability of each logic states was examined by a retiention measurement. At each states, the I_D of the memory OFET was measured at a bias voltage applied to S/D electrodes (V_D) of -60 V and a reading voltage applied to the gate (V_{read}) of -30 V. As shown in Fig. 3, all states were distinguished clearly after more 11.000 s of reading.

For conclusion, we demonstrate a multi-bit effect in the OFET using PCVN as charge trapping layer. More detail analysis and proposed mechanism operation of the memory will be reported in the presentation.

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Keywords: Charge trapping memory OFET, write-once-read-many memory, multi-bit memory

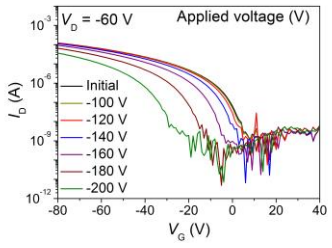

Fig. 1 Transfer characteristics of the OFETs under various programming voltages

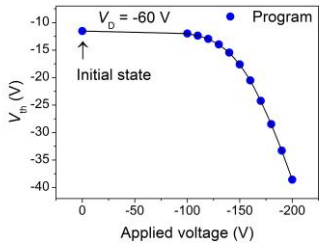

Fig. 2 The V_{th} of the OFETs as a function of negative programming voltages

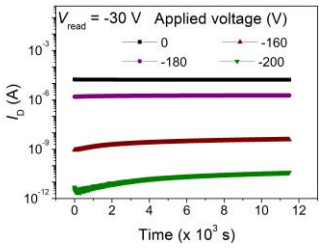

Fig. 3 Retention measurement of the memory