

Estimation of interface trap states density in Si(100)/MgO structure for spin injection into Silicon

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Spin transports between two ferromagnetic (FM) electrodes through semiconductor (SC) have been demonstrated by many groups using local/non-local Hanle and spin-valve measurements. However, the observed non-local spin signals were considerably smaller than predicted value from expected spin polarization of FM electrodes. The influence of interface trap states at the SC/Insulator interface on spin transport in real FM/Insulator/SC junction is not well understood [1]. In this work, we prepared Si(100)/MgO/Ta MOS capacitors with RF magnetron sputtering and EB evaporation methods and investigated interface trap state density for the high efficient spin injection into silicon. The films were deposited on p-type Si(100) wafers using ultrahigh vacuum magnetron sputtering and EB evaporation system ($P_{\text{base}} < 3.0 \times 10^{-6}$ Pa). Before loading in the chamber, all the substrates were dipped 1% HF for 3 min and ultra-pure water for 1 min. Then, the substrates were introduced in the chamber immediately, and flushed at 650°C for 10 min. The stacking structure of MOS capacitors were Si/ sputtered and EB evaporated MgO (20)/ Ta(10) and Si/ sputtered Mg(0.8)/ sputtered and EB evaporated MgO(19.2)/ Ta(10) (in nm). Both samples with and without post annealing were fabricated. The MOS capacitor devices were fabricated using photolithography and argon ion milling methods. The high frequency capacitance-voltage (CV) curves of Si(100)/MgO/Ta MOS capacitors measured at room temperature was shown in Fig. 1. The black line is the ideal CV curve calculated for same doping density and MgO thickness without interface traps [2]. The stretch out of experimental CV curves along gate voltage is corresponded to the interface traps occupancy change. Fig. 2 shows the interface traps density (D_{it}) versus gate voltage estimated from high frequency CV curves. EB evaporated samples demonstrated lower D_{it} than sputtered samples. The Mg inserted EB evaporated MgO sample with annealing (dark red box) formed the least trap state as $\sim 3 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ under the conduction band. It indicates that MgO tunneling barrier prepared by EB evaporation is greatly useful to decrease interface states in Si(100)/MgO/ferromagnet spin injection devices. This work was supported by ImPACT Program, grants-in-aid for scientific research S (No.24226001), and Interdepartmental Doctoral Degree Program for Multi-dimensional Materials Science Leaders of Tohoku Univ.

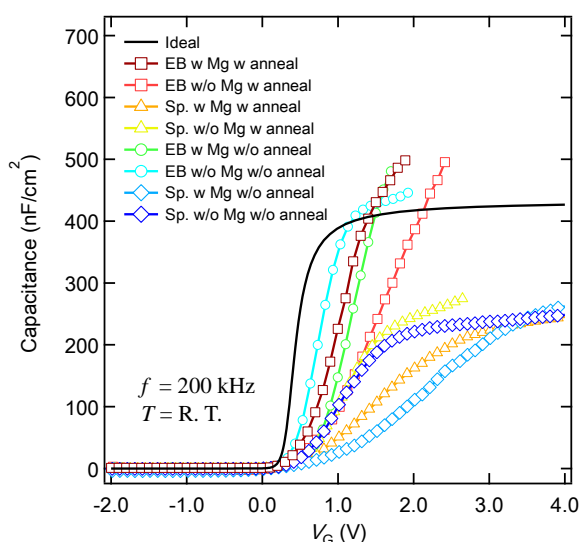


Fig. 1 High frequency capacitance-voltage curves of Si(100)/MgO/Ta MOS capacitors.

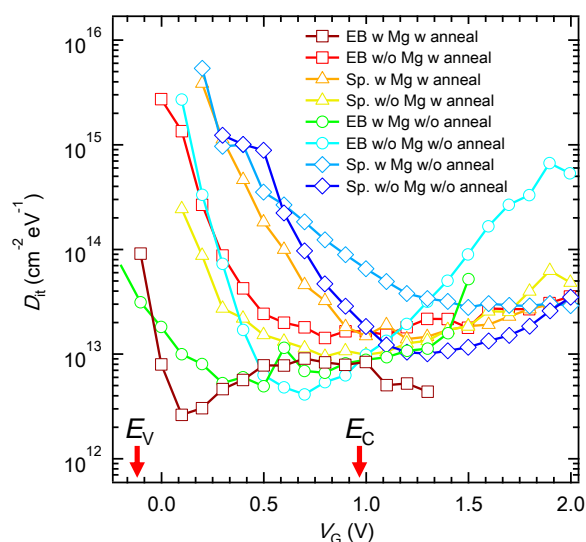


Fig. 2 Gate voltage dependence of interface states density (D_{it}) of Si(100)/MgO/Ta MOS capacitor

[1] F. Rortais *et al.*, Phys. Rev. B **94**, 174426 (2016).

[2] D. K. Schroder, Wiley, New York (1998).