

## Investigation on the trap states at p-GaN MO(I)S interface with different gate dielectric layers

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Recent progresses in the GaN-based electronic devices have demonstrated them as excellent candidates for the high power supply and switching systems, due to their unique characteristics, such as the high blocking voltage, wide bandgap, large electron saturation velocity and high thermal stability. Compared to Si or GaAs electronic devices, higher output currents can be achieved at higher frequencies by using GaN system. To fulfill the potential of GaN electronic devices, integration of GaN power devices and their gate driving circuits is needed to minimize the chip-to-chip parasitic inductance, thus reduce the switching loss, ringing and reliability issues. Monolithic complementary metal-oxide (insulator)-semiconductor (MO(I)S) transistors with both n-channel and p-channel for the integrated circuits is desirable to ultimately reduce the power consumption. However, the development of p-channel field effect transistors (FETs) is still in its infancy in comparison to the n-channel ones. Recently, our group has achieved p-channel MOSFETs based on polarization induced two dimensional hole gas at the InGaN/GaN heterojunctions. It is found that the performance of p-channel FET was restricted by the poor-quality p-GaN MOS interface[1-3]. As a result of Mg accumulation to the p-GaN surface, a large surface band bending of 1.2-1.6 eV was observed for the native p-GaN, which lead to in an interfacial Mg-Ga-O disordered region with high-density trap states on the order of  $10^{13} \text{ cm}^{-2}$  using  $\text{Al}_2\text{O}_3$  gate dielectric layer. The high-density traps resulted in the serious electrical hysteresis in both current-voltage (I-V) and capacitance-voltage (C-V) characteristic, bringing about the threshold voltage instability. The surface pre-treatment could not effectively remove the surface oxides on p-GaN as a result of re-oxidation in the following atomic-layer deposition process for  $\text{Al}_2\text{O}_3$ .

In this paper, we investigated the p-GaN MIS and MOS capacitors with different gate dielectric layer such as  $\text{CaF}_2$ ,  $\text{SiN}_x$ ,  $\text{SiO}_2$ , and  $\text{Al}_2\text{O}_3$ . The interface quality and traps behaviors are evaluated with regard to the microstructure and electrical characteristics. The oxide and oxygen-free gate dielectric layers were compared for the performance of p-GaN electronic devices.

### References

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