Challenges in 4H-SiC crystal growth and epitaxy for ultra-high voltage device applications

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Silicon Carbide is a promising material for low loss, high frequency and high voltage power device application, Especially, SiC power devices outperform conventional Si ones in term of low loss of electrical power and reducing device size of systems under ultra-high voltage ranges over 20kV. For example, Series connected Si Shyrister can be converted to single SiC IGBT. Then, feature electronic power transmission systems strongly require such devices.

The development of SiC IGBT strongly depends on material qualities of 4H-SiC bulk crystals and epitaxial layers. In generally, n-type drift layers grown on p-type substrate are used for n-channel IGBT. In this case, low resistivity p-type layer is applied as a drain region. However, conventional SiC p-type substrates have very high resistivity over 1 Ωcm and do not have enough high crystal quality. So that it is difficult for such substrates to use IGBT application. Then, past repots used high quality n-type substrates and p-type drift layers were grown on these substrates [1] or applied so-called flip type structure that n-type drift layers grown on these substrates and remove substrates [2]. These processes do not support enough IGBT operation characteristics and device manufacturing matching. Then, development of high quality and low resistivity p-type substrate with large diameter is required.

Other issues of SiC crystals for IGBT application is a growth of ultra thick epitaxial layer up to 300 μm thick for drift layers with long carrier lifrtime. For bipolar devices, enough long carrier lifetime is a key issue for low on resistance. In case of SiC, a concentration of deep level called $Z_{1/2}$ affects the carrier lifetime and deducing this concentration is very important. Off course, n-type epitaxial growth up to 300μm thick for 20kV blocking voltage devices is challenging issues itself. In addition, new dislocations have been generated at an interface between low resistivity p-type substrate and n-type drift layer because of the generation of high stress due to a lattice constant difference between high doped p-type substrate and low doped n-type drift layer. So, it needs to control the stress between them.

In this presentation, details of recent progress for growth of low resistivity 4H-SiC p-type substrates and thick epitaxial layer for IGBT applications will be presented.

[1] Z. Qingchun et al., IEEE Electron Device Lett., 29, 1027 (2008).

[2] Y. Yonezawa et al., Tech. Digest of 2013 Int. Electron Device Meeting, p. 6.6.1. (2013).

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