Very High Electrical Stability of Bottom-Gate/Top-Contact Type Polymer-Based Organic Field-Effect Transistors with Perfluoropolymer-Coated Gate Dielectrics

物材機構 [1]，筑波大数物 [2]，兵県大工 [3] ○(D2) ブルガレビッチ キリル [1,2]，坂本謙二 [1]，
三成剛生 [1]，安田剛 [1]，三木一司 [1,3]，竹内正之 [1,2]

NIMS [1], Univ. of Tsukuba [2], Univ. of Hyogo[3], ○Kirill Bulgarevich[1,2], Kenji Sakamoto[1], Takeo Minari[1], Takeshi Yasuda[1], Kazushi Miki[1,3], Masayuki Takeuchi[1,2]

E-mail: kirill.bulgarevich@nims.go.jp, sakamoto.kenji@nims.go.jp

Solution-processed organic field-effect transistors (OFETs) have important advantages over conventional silicon-based transistors, such as low-cost and low-temperature fabrication, suitability for large-area application, flexibility, and light weight. In addition to the field-effect charge carrier mobility, the long-term stability of OFETs is essential for commercial applications [1]. A hydroxyl-free amorphous perfluoropolymer, whose trade name is CYTOP (Asahi Glass Japan), is a promising gate dielectric or coating material for gate dielectric surfaces for fabricating electrically stable OFETs, because it is an excellent electrical insulator and shows a very high water-repellence. Indeed, high electrical stability has been reported for OFETs with CYTOP gate dielectric or CYTOP-coated gate dielectric [2]. However, for solution processing except for push-coating [3], the uniform deposition of active layers is difficult on such a highly lyophobic surface due to the dewetting of common organic solvents. Thus, there are few reports on the electrical characteristics of bottom-gate (BG) type polymer-based OFETs with CYTOP gate dielectrics or CYTOP-coated gate dielectrics. In this study, we developed a simple solution process to form uniform polymeric semiconductor layer on CYTOP-coated gate dielectric surfaces, and the electrical characteristics and bias-stress effect of polymer-based OFETs with CYTOP-coated gate dielectrics were carefully investigated under vacuum condition.

Poly(2,5-bis(3-hexadecylthiophene-2-yl)thieno[3,2-b]thiophene) (pBTTT-C16) was used as an active layer material. This is because it is a liquid crystalline polymer showing a smectic-like phase around 150°C and also because the CYTOP film works as a good homeotropic (vertical) alignment layer for smectic liquid crystals compared to long alkyl self-assembled monolayer surfaces [4]. BG/top-contact (TC) type OFETs shown in Fig. 1 were fabricated on CYTOP-coated and octadecyltrichlorosilane (ODTS)-treated SiO_2 (87 nm-thick)/n^+-Si(100) substrates. Both OFETs showed good p-channel OFET characteristics without drain current (I_d) hysteysis, and their initial electrical characteristics were similar to each other: $\mu \approx 0.3$ cm^2/Vs. However, very high operational stability against an on-state bias stress (V_{gs} = -30 V, V_{ds} = -1 V) was observed for the CYTOP-coated OFETs, compared to that of the ODTS-treated OFETs. By fitting the stress-time dependence of of I_d shown in Fig. 2 with a stretched exponential function [5], we estimated the stretching factor β and the trapping time constant τ. For the ODTS-treated OFETs, τ of the order of 10^7 s was observed (β =0.15). Assuming the same value of β, τ of the CYTOP-coated OFETs was several orders of magnitute larger than that of the ODTS-treated OFETs. The details of OFET fabrication process and data analysis will be presented at the conference.

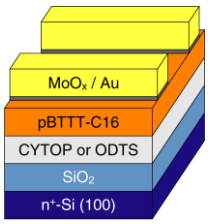

Fig.1 Device structure of OFETs fabricated in this study.

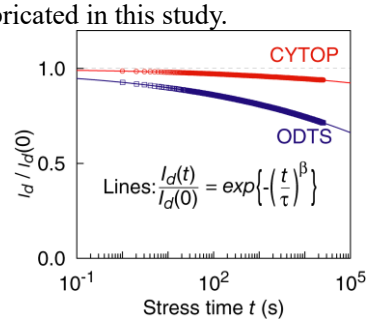

Fig. 2 Bias stress time dependence of normalized I_d for the pBTTT-C16 OFETs with CYTOP-coated (circles) and ODTS-treated (squares) SiO_2 gate dielectrics. The lines represent the fitting results with stretched-exponential functions.

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