4H-SiC m 面のウェット POA 条件の選択による MOS 界面準位密度の低減効果の違い

Effects of wet-POA with various conditions on 4H-SiC m-face MOS interface properties

[1] 東京大学大学院工学系研究科 マテリアル工学専攻，[2] (株)デンソー
○Qiao Chu[1]，山本 建策[2]，清水 皇[2]，喜多 浩之[1]
[1]The Univ. of Tokyo, [2]DENSO CORP. ◦Q. Chu[1], K. Yamamoto[2], S. Shimizu[2], and K. Kita[1]
E-mail: chu@scio.t.u-tokyo.ac.jp

[Introduction] Wet oxidation of SiC often results in significantly different MOS interface properties from dry oxidation [1,2]. We demonstrated on 4H-SiC Si-face, that the combination of dry oxidation and post-oxidation annealing in wet ambience (wet-POA) has a positive impact on MOSFET mobility [3]. For m-face, we also reported the reduction of MOS interface state density (D_{it}) by the same approach [4], but the impact of the selection of wet-POA conditions has not been clarified. In this research, we systematically investigated the effects of wet-POA with various conditions on m-face, focusing on D_{it} and bias stress instability.

[Experimental] N-type 4H-SiC m-face wafers (with epitaxial layer of N_D~6×10^{15} cm^{-3}) were oxidized under 1300°C in 2%O_2 for 15min, followed by dry annealing in N_2 for 5hrs. Next, wet-POA processes at 900°C were performed in various partial pressures of O_2 (pO_2) and that of H_2O (pH_2O) for different durations. SiO_2 layers with thickness around 15 nm were thermally grown by these combinations of processes. By depositing Au and Al layers, the capacitors were fabricated to measure the C-V characteristics.

[Results and Discussions] **Fig.1** shows the energy distributions of D_{it} below the conduction band edge, determined by conductance method, in various wet-POA conditions. D_{it} was significantly reduced by the wet-POA when pO_2 is low. The introduction of small amount of O_2 in wet-POA ambience, to achieve efficient reduction of D_{it}, is more beneficial than either without any O_2 introduction or high O_2 concentration; meanwhile, insignificant impact of pH_2O was found on D_{it} reduction. Note that expected thickness regrowth under low O_2 concentration ambience is only < 1 nm, even the wet-POA duration is up to 3 hours; while the case in high O_2 concentration ambience results in thickness regrowth ~ 3 nm for duration as short as 10 min. **Fig.2** shows the stress-time dependence of flatband voltage (V_{fb}) under constant positive gate voltage stress (3MV/cm) for samples fabricated in various wet-POA processes. As a result, reduction of pO_2 in wet-POA ambience improved V_{fb} stability under a positive gate bias. These results show that the O_2 content in ambience is an important factor to determine the POA effect on the annihilation of the traps at the interface, as well as the formation of traps in the oxide, for the formation of MOS interface on 4H-SiC m-face by wet oxidation.

[Conclusions] A significant reduction of D_{it}, down to 3×10^{11} $cm^{-2}eV^{-1}$ at 0.2 eV below the conduction band edge was demonstrated on 4H-SiC m-face, by dry oxidation followed by wet-POA at 900°C. The reduction of D_{it} was most pronounced for the wet-POA with a small O_2 content in the ambience, whereas the V_{fb} stability under a positive gate bias was improved by suppressing O_2 introduction to the wet-POA ambience.

References [1] M. Okamoto et al., Mater. Sci. Forum 778-780, 975 (2014). [2] H. Hirai and K. Kita, APL 110, 152104 (2017). [3] H. Hirai and K. Kita, ICSCRM (2017, Washington DC). [4] K. Kuroyama et al., JSAP Spring Meeting (2017, Yokohama).

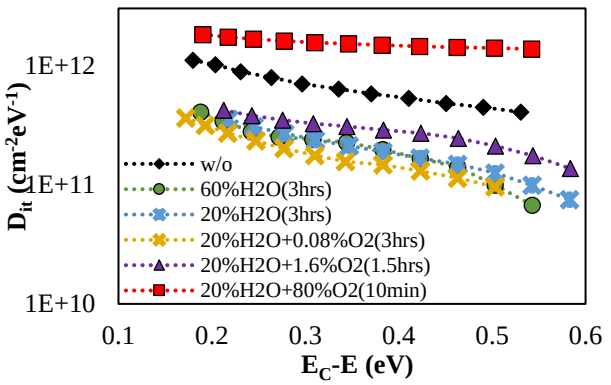

Fig. 1 Energy distribution of D_{it} of 4H-SiC m-face MOS capacitors fabricated with combined processes of same dry oxidation and various wet-POA conditions.

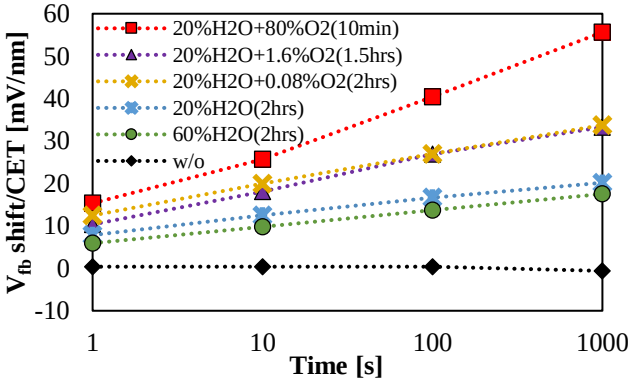

Fig. 2 Stress-time dependence of V_{fb} under constant voltage stress (3MV/cm) for the sample fabricated with dry-oxidation followed by wet-POA in various conditions.