Low-temperature fabrication of Ge MOS capacitors for spintronics and flexible electronics application

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Introduction

Ge is of great interest in MOSFET applications due to its high carrier mobilities. Many issues have been solved, and high mobility Ge MOSFETs have been reported. [1,2] Another possible application ways of Ge are spintronics (spin-FET) and flexible electronics (high mobility TFT on polymer substrate). [3,4] For such applications, a low temperature fabrication process is necessary because of the low thermal stability of spin-source/drain or polymer substrate. However, no one has focused fabrication of high quality Ge MOS at low temperature yet. In this study, we aim to investigate qualities of Ge MOS capacitors (CAPs) fabricated under low temperatures.

Experimental

Both p- and n-type (111) Ge substrate with doping concentration 1.2×10^{16} and 4.0×10^{15} cm^{-3} was used. The reason we used (111) surface is that spin injection/detection electrodes can be formed on (111) surface. [3] After wet cleaning, SiO_2/GeO_2 bilayer passivation (BLP) was performed at 250°C. [5] Then, 10 nm SiO_2 was deposited at room temperature, and a post- deposition annealing (PDA) at 250°C in N_2 ambient for 30 minutes was carried out. Next, Al/TiN are deposited and patterned as electrodes. Finally, a post- metallization annealing (PMA) was performed at 250°C in N_2 ambient for 30 minutes, followed by a back contact formation. In order to compare the performance to the MOSCAPs fabricated at higher temperatures, the other MOSCAPs were fabricated with the same process, but both BLP and PMA temperatures were 300°C. In addition, the PDA temperatures were 300°C, 350°C and 400°C, respectively. Thermal budgets for the processes of all the MOSCAPs are shown in Fig. 1.

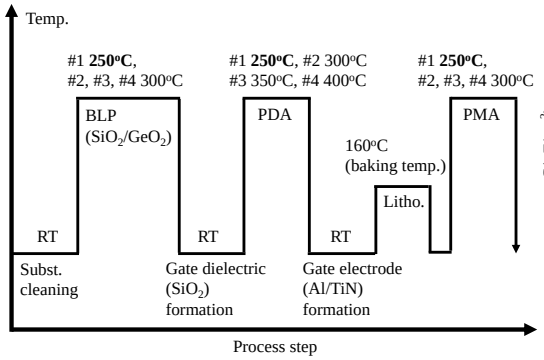

Fig. 1 Thermal budgets.

Results and discussion

Figure 2 shows the *C-V* characteristics of MOSCAPs fabricated under 250°C. Typical *C-V* curves were obtained, and they are not different from those fabricated under high temperatures (not shown). The small hysteresis implies the border traps concentration is low. Besides, the high breakdown electric field indicates that the leakage current is well suppressed (figures are not shown). *C-V* and *I-V* characteristics and D_{it} of all the MOSCAPs will be presented in the conference.

Conclusion

We successfully fabricated Ge MOSCAPs under 250°C, which is low enough to apply to spin-FET and flexible electronics. Although the performance may need to be improved, it seems Ge has potential for advanced applications.

References

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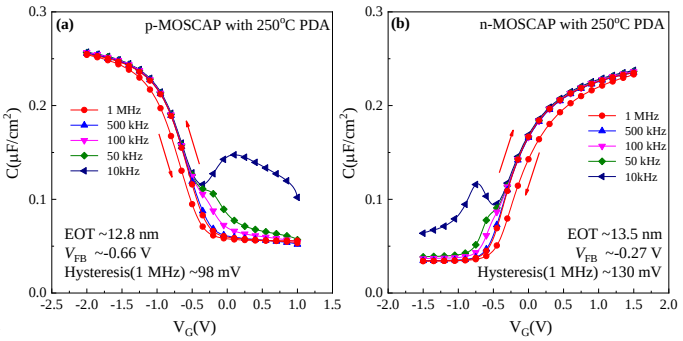

Fig. 2 *C-V* characteristic of (a) p-MOSCAP and (b) n-MOSCAP fabricated under 250°C.