

結晶 Si/PEDOT:PSS 太陽電池における界面局所電界強度の増強効果

Photovoltaic performance of PEDOT:PSS/c-Si junction solar cells by adding ferroelectric polymer thin-layer

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1. Introduction: We have investigated the effect of solution derived ferroelectric (FE) layer P(VDF-TrFE) on the front-PEDOT:PSS/Si junction solar cells. In particular, the open circuit voltage (V_{oc}) corresponding to the built-in potential is increased from 525 mV to 531 mV by inserting the FE layer (~6 nm) between PEDOT:PSS/Si interface and farther improved to 561 mV by inserting FE at rear Si/cathode interface. In addition, the PCE is also enhanced from 9.83% to 11.53%.

2. Experimental: The solar cells are fabricated on n-Si (250μm thick 0.1~0.5 Ω-cm resistivity 1×1 cm²) substrate. After the RCA cleaning of the substrate, a thin layer (~6nm) of the FE polymer is spin coated (SC) on top or/and back side of the n-Si substrate followed by thermal annealing at 100°C for 10min. After that, a ~100-nm-thick PEDOT:PSS is coated and heat treated at 140 °C for 30 min. Then, the upper Ag grid and the back Al electrodes are provided as anode and cathode.

3. Results and discussion: Fig. 1(a) shows the $1/C^2-V$ characteristics of the PEDOT:PSS/n-Si interface together with FE layer insertion. The built-in potential (ψ_{bi}) is determined by the linear extrapolation of the $1/C^2-V$ graph. It's increased from 0.79 V to ~0.86 V by inserting ~6nm FE layer at cathode interface. The enhanced ψ_{bi} indicates the increasing of internal electric field provided by the spontaneous polarization of FE polymer. Fig. 1(b) shows $J-V$ curves of the PEDOT:PSS/n-Si solar cells with and without FE layer. The induced electric field by FE layer contribute to improve carrier collection ability as well as V_{oc} and PCE as observed in $J-V$ characteristics. We will discuss the effect of bias poling and thermal annealing on photovoltaic performance.

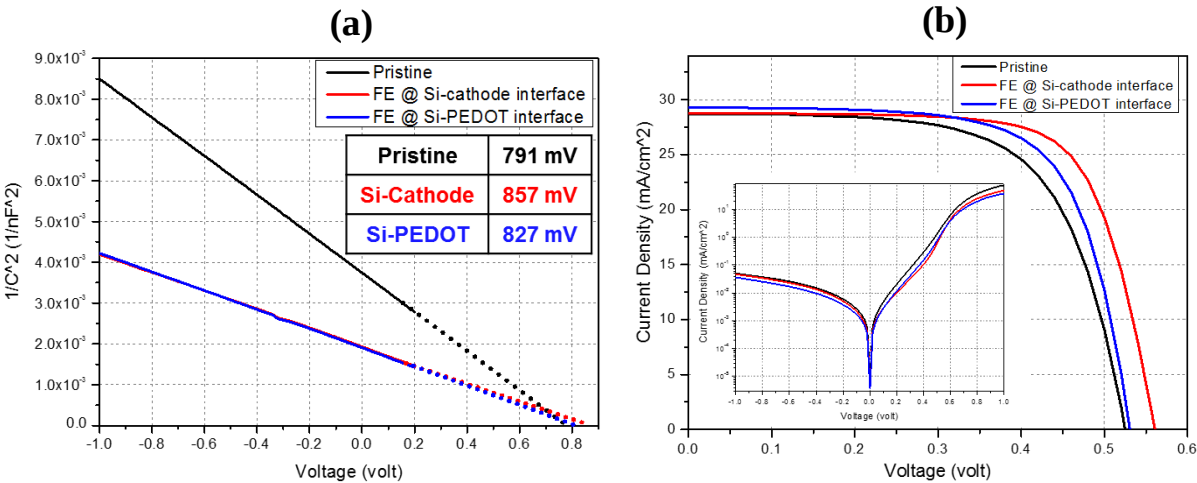


Fig.1: (a) C-V and (b) J-V characteristics of the PEDOT:PSS/n-Si solar cell with and without FE layer.