多接合太陽電用 GaAs 系トンネルダイオードの MOVPE 成長
MOVPE growth of GaAs-based tunneling diode for multiple junction solar cells

◦ソダーバンル・ハッサネット [1],, 渡辺健太郎 [1], 杉山正和 [1-2], 中野義昭 [2]
◦ H. Sodabanlu[1], K. Watanabe[1], M. Sugiyama[1-2], Y. Nakano[2]
[1] 東大先端研 RCAST, The Univ. of Tokyo, [2] 東大院工 School of Engineering, The Univ. of Tokyo
◦E-mail: sodabanlu@hotaka.t.u-tokyo.ac.jp

1 Introduction

The recent record conversion efficiency of 46% has been realized by InGaP/GaAs/InGaAsP/InGaAs 4-junction (4J) solar cells fabricated by direct wafer bonding technique [1]. Our group reported in this community about the optimization of metalorganic vapor phase epitaxy (MOVPE) growth for InGaAsP/InGaAs dual junction solar cells [2]. In this work, we investigated and optimized the growth conditions for GaAs-based tunneling diodes (TDs) for InGaP/GaAs electrical interconnection as a further step toward the fabrication of 4J solar cells.

2 Experimental details, results and discussion

The experiment was carried out using a planetary MOVPE reactor. Due to the limitation of our MOVPE system, the dopant sources for n-type and p-type doping were limited only to diethyltelluride (DETe) and dimethylzinc (DMZn), respectively. The investigated structure consisted of 500-nm-thick p-GaAs contact layer on p+/n+ GaAs TDs, 100-nm-thick each, and 500-nm-thik n-GaAs buffer grown on (001) n-GaAs substrates (Si 2x10^{18} cm^{-3}). The in-situ surface temperature of GaAs wafer was observed by emissivity-corrected pyrometry. First, two GaAs TDs were fabricated using the identical growth conditions excepting that the first sample was grown with a standard surface temperature of 600 ºC and the other one with a temperature of 570 ºC.

Figure 1(a) shows the profiles of active carrier concentration in GaAs TDs evaluated by electrochemical capacitance-voltage measurement. Obviously, by decreasing the surface temperature, the carrier concentrations of both Te and Zn doped GaAs could be greatly enhanced. These results can be explained by a decrease in dopant desorption from GaAs surface at a lower temperature. Applying these carrier profiles to a simulation, the energy band diagrams of both samples were calculated and plotted in Fig. 1(b). Owing to higher carrier concentrations, the junction width between p+ and n+ GaAs was clearly narrower in the case of 570 ºC grown sample. After depositing metal electrodes, the samples were mesa-etched to have an area of 4.7 mm^2. The current-voltage (I-V) characteristics of both GaAs TDs were plotted in Fig. 1(c). Note that, the current was limited to 0.1 A in this measurement, and the peak tunneling current could not be evaluated here. Nevertheless, the 600 ºC grown TD obviously exhibits a diode behavior, while the other has ohmic like I-V curve with a sheet resistivity of 14 mΩ•cm^2. Further studies and optimizations have been under investigation including the implementation of wide bandgap materials, and growth parameters.

3 Summary

The low temperature growth is proved to be beneficial for the growth of highly doped GaAs-based TDs. Further studies and optimizations have been under investigation.

A part of this study was supported by New Energy and Industrial Technology Development Organization (NEDO).

[1] F. Dimroth et al., J. Photovoltaics **6**, 343, 2016.
[2] H. Sodabanlu et al., 78th JSAP, 7p-S21-15, 2017

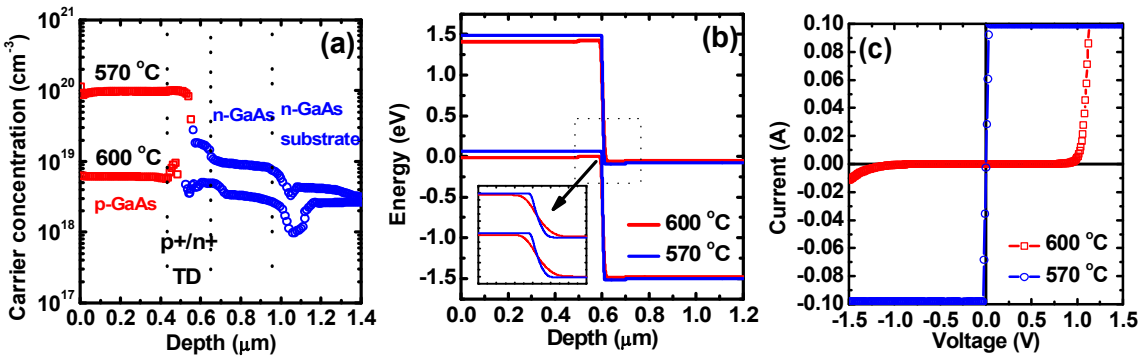

Fig. 1 (a) Carrier profiles of GaAs TDs grown at different temperatures (b) band diagrams simulated using data from Fig. 1(a) and (c) current-voltage curves of GaAs TDs grown at different temperatures