Ultralow Latency Computation based on Integrated Nanophotonics

Masaya Notomi^{1,2}, Kengo Nozaki^{1,2}, Shota Kita^{1,2}, Akihiko Shinya^{1,2}, Tohru Ishihara³, Koji Inoue⁴

NTT Basic Research Laboratories, 2) NTT Nanophotonics Center,
3) Kyoto University 4) Kyushu University

E-mail: notomi.masaya@lab.ntt.co.jp

Moore's law for CMOS computers is still continuing, but its near-future saturation is now being discussed. One of the serious saturations is about its latency. The computation delay for a CMOS transistor is already saturated above 10 ps, which will be problematic when ultralow-latency response is required for broad-band data streams, even with parallelization or pipe-line processing. We regard that optical circuits may serve as ultralow-latency computation circuits if they are small enough and tightly combined with electronic circuits. The former requires nanophotonic devices/circuits and the former requires OE/EO conversion with ultrasmall capacitance.

In this talk, first, we present our recent achievement in OE/EO conversion devices having significantly small capacitance. Then, we show that if we adopt a certain type of logic where the computation delay is governed by the path delay (optical pass-gate logic), ultralow-latency computation will be possible using nanophotonic circuits. We show several examples including optical full-adder circuits consisting of electro-optic switches and digital-to-analogue converters, some Boolean logic circuits based on linear optic elements, verctor-matrix multiplication for neuromorphic computing.

This work is partly supported by CREST (#JPMJCR15N4), JST.