Effects of the impurity concentration in the Ge sources on the electrical properties of Ge/Si TFETs

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1. Introduction A Ge-source/Si-channel hetero-junction TFET is a promising device structure because of the type-II staggered band alignment between Ge and Si [1-2]. Here, the smaller bandgap of the Ge-source and the band-offset of the hetero-junction can increase the tunneling possibility. In this TFET structure, the source impurity concentration, which determines the depletion width and the resulting tunneling distance, is a critical factor to enhance the electrical characteristics [3]. However, the source concentration dependence in the Ge/Si TFETs has not been sufficiently studied yet. In this study, we have first experimentally analyzed the effects of the impurity concentration in the Ge sources on the electrical properties of Ge/Si TFETs.

2. Experimental Results and Discussion Fig. 1 shows the schematic process flow of the Ge/Si hetero-junction TFETs. Here, a key process parameter is the source doping concentration. Thus, the B concentration doped in Ge is varied from 1×10^{18} to 1×10^{20} cm^{-3} in order to evaluate the effects on the Ge/Si TFET performance. Fig. 2 (a) shows the Raman spectra of the B-doped Ge epitaxial layers with different B concentrations. The peak for the B-doped epitaxial layer with the highest B concentration is shifted toward the lower wave number and the full width at half maximum is broadened. These are attributable to a coherent interference between a discrete phonon line and continuum inter-band hole excitations, observed in degenerately-doped p-type Ge [4]. The impurity concentration dependence of the Fermi level (E_F) in Ge (Fig. 2 (b)), calculated by using the Fermi-Dirac distribution function, shows that the doping of 1×10^{20} cm^{-3} makes E_F lower than the valence band edge. Fig. 3 shows the I_D-V_G curves of the fabricated devices. It is found that I_{on} and SS are significantly affected by the B concentration in Ge. The steep SS of 63.8 mV/dec and large I_{on}/I_{off} ratio of 5.7×10^6 are obtained for the source doping concentration of 9×10^{18} cm^{-3}. Fig. 4 summarizes I_{on} and SS as a function of the source doping concentration. The higher source doping concentration is supposed to decrease the depletion width and increase the tunneling probability [3]. It is found, however, that the highest B concentration of 1×10^{20}cm^{-3} degrades SS, attributable to the depression of the energy filtering effect in the band edge between Ge and Si by the degenerated E_F position, shown in Fig. 2(b), under such high B concentrations [5]. Fig. 5 shows the SS increment as a function of temperature. The strongest temperature dependence of SS is observed for TFETs with the highest B concentration of 1×10^{20} cm^{-3}, which can be a direct evidence of the SS degradation due to the depression of the energy filtering effect. This is because the degenerated E_F in the high source concentration yields the exponential tail of the energy distribution of holes inside the valence band. Such an energy distribution can weakens the rapid increase in tunneling current through the overlapping the density of states between the conduction and the valence bands [5].

3. Conclusion The effects of the Ge-source impurity concentration on the electrical characteristics of Ge/Si TFETs were experimentally studied. The source concentration of 9×10^{18} cm^{-3} has been found to be optimal for steep SS. The degradation in SS with higher source concentrations is explained by the depression of the energy filtering effect due to the degeneracy of E_F, which has been supported by the temperature dependence of SS.

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References [1] O. M. Nayfeh et al., EDL 29 (2008) 1074 [2] M. Kim et al., TED 62 (2015) 9 [3] G. Han et al., Appl. Phys. Lett., 98 (2011) 153502 [4] F. Cerdeira et al., Phys. Rev. B, 5 (1972) 1440 [5] J. Knoch et al., EDL 31 (2010) 305

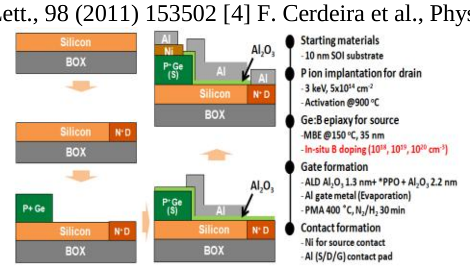

Fig. 1 Process flow of the Ge/Si TFETs

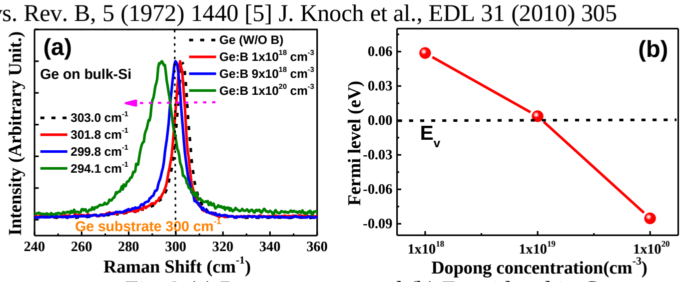

Fig. 2 (a) Raman spectra and (b) Fermi level in Ge

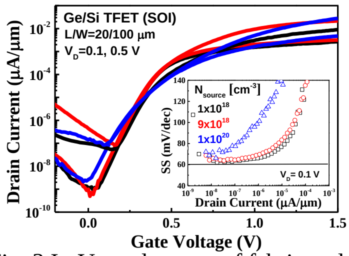

Fig. 3 I_D-V_G and curves of fabricated devices

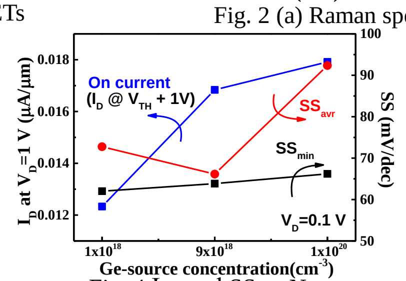

Fig. 4 I_{on} and SS vs N_{source}

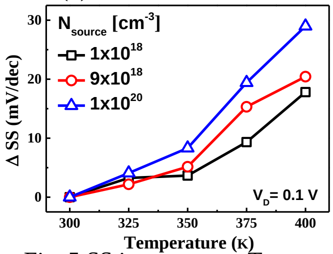

Fig. 5 SS increment vs Temperature