Initial trap and hysteresis analysis of Atomic Layer Deposited Al_2O_3 on β-Ga_2O_3

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Introduction

Recently, beta gallium oxide (β-Ga_2O_3) caught attention as one of the most promising prospect for high-voltage power device applications due to its excellent material properties [1]. The most impressive material property of Ga_2O_3 is a wide bandgap of 4.7~4.9 eV. with a breakdown electric field 8 MV/cm, which is about three times larger than those of SiC and GaN power device materials. The fact that large area single crystal substrates can be fabricated from melt-grown bulk crystals can be another significant advantage of Ga_2O_3, and the edge-defined film-fed growth (EFG) method, which is one of the low cost methods, has already been applied to produce large sapphire wafers. Since it does not require a high temperature or high-pressure environment and conserves source material, Ga_2O_3 wafers will be especially useful for low-cost mass production. Along with the reports on high voltage Schottky diodes, MOS transistors have now been reported. In this research, atomic-layer-deposited (ALD) Al_2O_3 with a thickness of 40 nm has been used as a gate dielectric [2]. The initial trap and C-V hysteresis will be investigated.

Experiment

A 40-nm-thick-Al_2O_3 gate dielectric film was deposited by ALD on the surface of a Ga_2O_3 substrate with n-type epitaxial layer. The doping density (N_d) of the epitaxial layer was 2.3×10^{16} cm^{-3}. The sample was transferred to a sputter chamber and 50-nm-thick W film followed by 50-nm-thick TiN was deposited by RF magnetron sputtering as a gate electrode. The capacitor was patterned by reactive ion etching (RIE) to form gate electrodes. Finally, a 10-nm-thick Ti followed by a 50-nm-thick TiN was deposited on the backside of the substrate as an Ohmic contact, followed by 30-min annealing at 400°C in a forming gas (3% H_2, 97% N_2) atmosphere by using a rapid thermal annealing (RTA) system. Figure 1 shows the schematic illustration of the fabricated MOS capacitor.

Results and discussion

The first and second measured C-V curves are shown in figure 2. A double sweep measurement was performed starting from -20V to 5V. A wide clockwise hysteresis of 0.85 V measured at the first sweep was reduced to 0.3 V. which indicates there are initial electron trapping in addition to the border traps. Figure 3 shows the magnitude of initial and hysteresis voltages with different turn-back voltage during the sweeps. From the intercept, the border traps for hysteresis can be considered to locate at the interface of Al_2O_3/Ga_2O_3, whereas the stored traps that are located inside the Al_2O_3.

Conclusion

Initial trap and hysteresis will impact on positive gate voltage. As a result of this, we can speculate that the charge will be captured on the surface of Al_2O_3 dielectric layer reasonably. And the number of captured charge positively correlated with the gate voltage.

References

[1] M. Higashiwaki et al., Appl. Phys. Lett, **103**, 123511 (2013)
[2] Takafumi Kamimura et al., *Jpn. J. Appl. Phys.* **55** 1202B5 (2016)

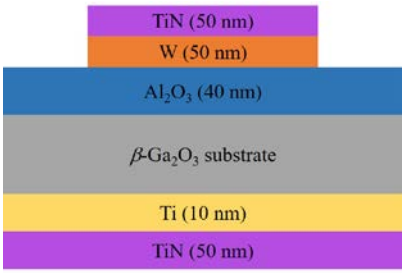

Fig.1 Cross section of MOS capacitor.

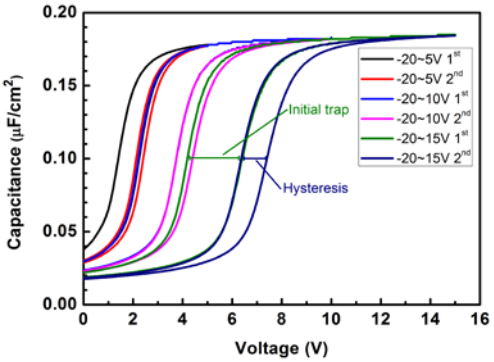

Fig. 2 Capacitor and voltage characteristic measure under 1MHz

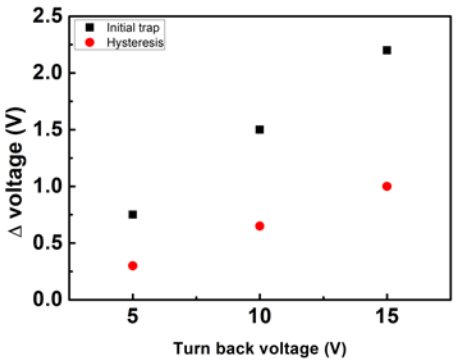

Fig. 3 Initial trap and C-V hysteresis analysis