Initial trap and hysteresis analysis of Atomic Layer Deposited Al₂O₃ on β-Ga₂O₃


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Introduction
Recently, beta gallium oxide (β-Ga₂O₃) caught attention as one of the most promising prospects for high-voltage power device applications due to its excellent material properties [1]. The most impressive material property of Ga₂O₃ is a wide bandgap of 4.7~4.9 eV, with a breakdown electric field 8 MV/cm, which is about three times larger than those of SiC and GaN power device materials. The fact that large area single crystal substrates can be fabricated from melt-grown bulk crystals can be another significant advantage of Ga₂O₃, and the edge-defined film-fed growth (EFG) method, which is one of the low-cost methods, has already been applied to produce large sapphire wafers. Since it does not require a high temperature or high-pressure environment and conserves source material, Ga₂O₃ wafers will be especially useful for low-cost mass production. Along with the reports on high voltage Schottky diodes, MOS transistors have now been reported. In this research, atomic-layer-deposited (ALD) Al₂O₃ with a thickness of 40 nm has been used as a gate dielectric [2]. The initial trap and C-V hysteresis will be investigated.

Experiment
A 40-nm-thick Al₂O₃ gate dielectric film was deposited by ALD on the surface of a Ga₂O₃ substrate with n-type epitaxial layer. The doping density (N_d) of the epitaxial layer was 2.3×10¹⁶ cm⁻³. The sample was transferred to a sputter chamber and 50-nm-thick W film followed by 50-nm-thick TiN was deposited by RF magnetron sputtering as a gate electrode. The capacitor was patterned by reactive ion etching (RIE) to form gate electrodes. Finally, a 10-nm-thick Ti followed by a 50-nm-thick TiN was deposited on the backside of the substrate as an Ohmic contact, followed by 30-min annealing at 400°C in a forming gas (3% H₂, 97% N₂) atmosphere by using a rapid thermal annealing (RTA) system. Figure 1 shows the schematic illustration of the fabricated MOS capacitor.

Results and discussion
The first and second measured C-V curves are shown in figure 2. A double sweep measurement was performed starting from -20V to 5V. A wide clockwise hysteresis of 0.85 V measured at the first sweep was reduced to 0.3 V, which indicates there are initial electron trapping in addition to the border traps. Figure 3 shows the magnitude of initial and hysteresis voltages with different turn-back voltages during the sweeps. From the intercept, the border traps for hysteresis can be considered to locate at the interface of Al₂O₃/Ga₂O₃, whereas the stored traps that are located inside the Al₂O₃.

Conclusion
Initial trap and hysteresis will impact on positive gate voltage. As a result of this, we can speculate that the charge will be captured on the surface of Al₂O₃ dielectric layer reasonably. And the number of captured charge positively correlated with the gate voltage.

References