

Simulation of Heat Extraction from Ga₂O₃ MOSFETs with an Integrated SiC Heat Sink

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Wide-bandgap β -Ga₂O₃ has attracted considerable interest for power electronics, but its low thermal conductivity of less than 30 W/m·K limits the performance and reliability of Ga₂O₃ devices. A common approach to address self-heating in high power transistors involves integrating active device layers with a thermally conductive foreign substrate for heat extraction. As a proof of concept, we performed electrothermal simulations in this work to demonstrate the effectiveness of polycrystalline SiC (poly-SiC) as a heat sink material for reducing the channel temperature and improving the DC characteristics of Ga₂O₃ power devices.

A prototype design of 3.3-kV normally-on vertical Ga₂O₃ metal-oxide-semiconductor field-effect transistors (MOSFETs) was employed in this study (Fig. 1). 2-D electrothermal simulations of devices built on either an n^+ -Ga₂O₃ or n^+ -poly-SiC substrate were performed using Silvaco ATLAS. A temperature dependence of $T^{-1.5}$ was implemented for bulk electron mobilities. Experimental temperature-dependent anisotropic thermal conductivities were adopted for Ga₂O₃ [1], whereas an isotropic value of 330 W/m·K with an estimated $T^{-1.3}$ dependence was used for poly-SiC [2,3]. Heat dissipation from the device to the ambient (27°C) was modeled by imposing isothermal boundary conditions at the source and drain ohmic contacts; all other surfaces were adiabatic. Thermal boundary resistance between Ga₂O₃ and poly-SiC, which typically arises from nucleation layers and/or defects at real interfaces, was not considered. The same electrical resistivity (0.02 Ω ·cm at 27°C) was applied to both Ga₂O₃ and poly-SiC substrates so that differences in device characteristics could be attributed solely to thermal effects.

Improved thermal performance of the Ga₂O₃/poly-SiC MOSFET compared to its Ga₂O₃/Ga₂O₃ counterpart was evident from the relationships between peak device temperature (T_{pk}) and DC power dissipation (P_D) (Fig. 2). The average thermal resistance, defined as the temperature rise per unit P_D and determined by linear fitting to the T_{pk} vs. P_D data, was lower for the Ga₂O₃/poly-SiC device by more than 50%. Enhanced heat extraction by poly-SiC reduced the T_{pk} in the Ga₂O₃ channel from 340°C to 175°C at $P_D = 4$ W/mm. As a direct consequence of reduced self-heating, the Ga₂O₃/poly-SiC MOSFET delivered a 42% increase in saturated drain current (I_{DS}) and a 72% improvement in peak transconductance (g_m) at a drain/gate bias [V_{DS} , V_{GS}] = [30 V, 0 V] (Fig. 3).

This work was partially supported by Council for Science, Technology and Innovation (CSTI), Cross-ministerial Strategic Innovation Promotion Program (SIP), “Next-generation power electronics” (funding agency: NEDO).

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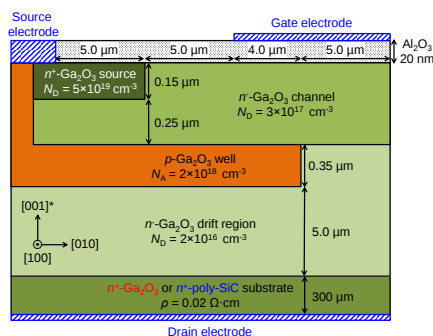


Fig. 1. Cross-sectional schematic of a vertical Ga₂O₃ MOSFET unit cell. The simulation domain consisted of two unit cells symmetric about its vertical midline.

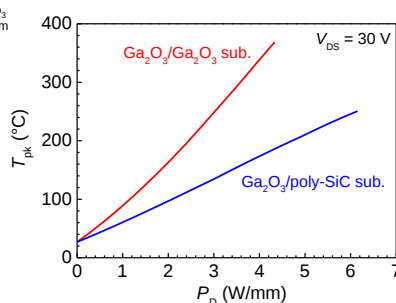


Fig. 2. T_{pk} vs. P_D (per unit gate width) of the Ga₂O₃/Ga₂O₃ and Ga₂O₃/poly-SiC MOSFETs showing lower thermal resistance for the latter.

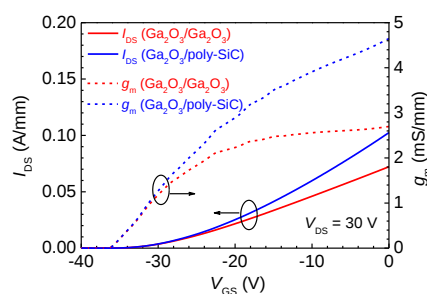


Fig. 3. Transfer characteristics showing improved electrical characteristics of the Ga₂O₃ MOSFET on a poly-SiC heat sink.