# Current Aperture Vertical $Ga_2O_3$ MOSFETs with N-Ion-Implanted Current Blocking Layer

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Vertical power transistors are preferred over their lateral counterparts since chip area utilization is more efficient and device operation is insensitive to surface effects. A current aperture vertical $Ga_2O_3$ metal-oxide-semiconductor field-effect transistor (MOSFET) was previously demonstrated, wherein the source was isolated from the drain by an Mg-doped current blocking layer (CBL) except at an aperture opening through which drain current ($I_{DS}$) was conducted [1]. In this work, an N-doped CBL was adopted for FET fabrication in light of its higher thermal stability and larger blocking voltage than with Mg doping [2].

The vertical $\beta$-$Ga_2O_3$ MOSFET (Fig. 1) consisted of a 6-µm-thick Si-doped ($3\times10^{16}$ $cm^{-3}$) $n^-$-$Ga_2O_3$ drift layer grown by halide vapor phase epitaxy (HVPE) on an $n^+$-$Ga_2O_3$ (001) substrate [3]. The buried CBL was formed by N-ion ($N^{++}$) implantation doping. To recover implantation damage and activate N as a deep acceptor, thermal annealing was performed at 1100°C for 30 min in $N_2$. Contrary to the case for Mg, annealing temperatures above 1000°C can be employed for N to enhance implant activation without causing significant dopant diffusion [2]. Subsequent Si-ion ($Si^+$) implantations defined the electron channel and $n^+$ source contacts. A 50-nm-thick $Al_2O_3$ gate dielectric was then formed by plasma-assisted atomic layer deposition. Ti/Au and Ti/Pt/Au were used for the ohmic and gate electrodes, respectively. Device fabrication was completed with deposition of Ti/Au source probing pads on $Al_2O_3$ for low pad leakage.

The resistivity of the CBL was characterized using vertical two-terminal test structures. A leakage current of 1 mA/cm$^2$, which corresponded to typical on/off current ratios of $10^5$-$10^6$, was registered at biases of 10-40 V (Fig. 2). The nonlinear current-voltage characteristics attested to the formation of an electron barrier across the $N^{++}$-implanted CBL. Carrier depth profiling by capacitance-voltage measurements in regions without a CBL revealed full Si activation in the channel; however, a very low $I_{DS}$ of ~100 mA/cm$^2$ was measured in a MOSFET with a gate-CBL overlap ($L_{go}$) of 5 µm despite a large aperture opening ($L_{ap}$) of 25 µm (Fig. 3), which unequivocally pointed to a resistive channel above the CBL. The loss of carriers, which could be ascribed to remnant compensating defects from $N^{++}$ implantation, the N profile being shallower than expected, and/or depletion by an electrostatic potential at the channel/CBL junction, will be addressed in subsequent work.

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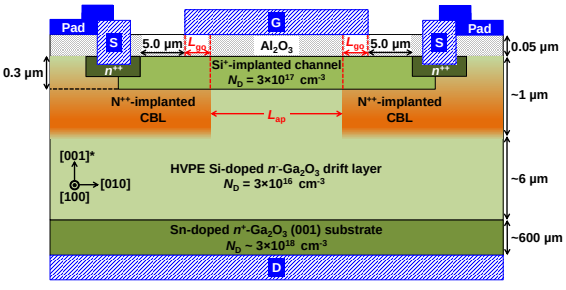


Fig. 1. Cross-sectional schematic of the vertical $Ga_2O_3$ MOSFET. The aperture and source widths were 200 µm.

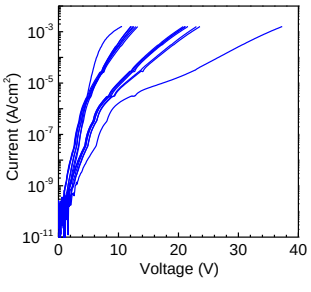


Fig. 2. Vertical leakage through the $N^{++}$-implanted CBL.

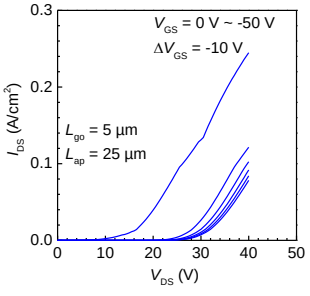


Fig. 3. DC $I_{DS}$-$V_{DS}$ characteristics of the vertical $Ga_2O_3$ MOSFET.