Impact of solid-state memristor variability on perceptron supervised learning via STDP

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Memristors [1] are non-volatile memory elements with an electrically programmable resistance. Bipolar binary memristors have extensive promise in replacing FLASH as the next generation storage/memory medium. Conversely we focus here on bipolar *analogue* memristors (with a continuously variable resistance), which represent promising candidates for implementation as artificial synapses in hardware-based artificial neural networks towards realisation of power efficient and compact neuromorphic processors [2]. These have impactful applications in the design of autonomous cognitive agents [3] and deep-learning accelerators [4]. However progress in this field has been hindered by practical device issues.

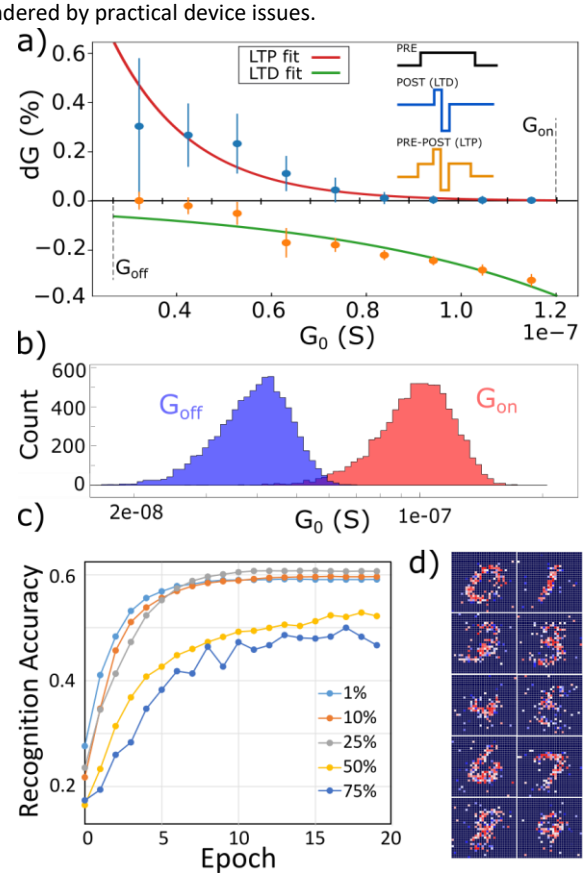

Figure 1: a) Behavioral memristor model responding to LTP- and LTD-inducing pulse shapes. b) Example of initial conductance distributions c) Degradation of perceptron recognition accuracy due to initial conductance variation. d) Output neurons receptive fields after training for 25% initial conductance variation.

As has been extensively reported, solid-state analogue memristors suffer from large variability in their operation metrics, namely resistive state dynamic range and switching kinetics [5]. In this paper, we implement in simulation a single layer perceptron using a behavioural model of practical analogue memristors for the role of synapses (Figure 1a), and quantify the effect of device non-idealities on the network's performance. The perceptron is implemented as a fully interconnected input and output neuron layers, with two memristor crossbars emulating the role of excitatory and inhibitory synapses in order to achieve both negative and positive conductances between any two arbitrary input and output neurons. We train the perceptron on a constrained MNIST dataset to recognise hand written digits. We implement a Hebbian-like custom pulse-based learning rule inspired by Spike-timing dependent plasticity (STDP) observed in biological synapses [6]. This can be simply summarised as: if both input (PRE) and output (POST) neurons are active, the corresponding synapse needs to be potentiated (Long-term potentiation – LTP); if only the output neuron (POST) is active, the corresponding synapses need to be depressed (Long-term depression – LTD); in any other case, no change occurs. This is achieved by the pulse shapes in Figure 1a (inset) applied to excitatory synapses while inhibitory synapses receive inverted pulse shapes. This "blind" (no READ check) synapse update mechanism accelerates the learning time, and is more suitable for synapses characterized by multiplicative STDP [7], such as our model suggests.

We explore, via simulation, how the recognition accuracy and classification speed of this perceptron degrades when taking into account noise and realistic memristive device variability (Figure 1b). We highlight device metrics which strongly influence the network's performance (Figure 1c,d) and hence require design attention from device engineers. Although this work only takes into account a single layer perceptron, the performance degradation of multi-layer perceptrons trained via STDP can be inferred from similar simulations.

[1] Chua, L, Applied Physics A **102**, issue 4, pp 765-783, 2011.
[2] Indiveri, G., et. Al., Nanotechnology **24,** 384010, pp 1-13, 2013.
[3] Shuman, D., C., et. al., arXiv:1705.06963v1, 2017.
[4] Burr, G. W, et. al., IEEE Trans on Electron Devices **62**, 2015.
[5] Kim, M. K, et. al., Nanotechnology **22**, 254002, 2011.
[6] Serb, A. et. al., Nature Communications **7**, 12611, 2016.
[7] Serrano-Gatarredona, T. et. al., Front. Neurosci **7:2**, 2013.