Why don't you enjoy Ge CMOS more?

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1. Introduction

Ge used to be intensively investigated before 1960. Why Ge was beaten by Si? There were a couple of reasons in terms of (i) junction leakage, (ii) material volume, (iii) gate stack challenges, etc. Now we are tackling with Ge again (*). We have to understand merits and demerits of Ge, and to differentiate between intrinsic challenges and optimization issues. Otherwise, Ge is "the next generation material" forever. The mobility in bulk Ge is usually addressed as the big merit of Ge, however, there is a big discrepancy of the mobility between in the bulk and at the interface even in Si. To enjoy the merit, it is beyond question that the interface quality control is the key. Since interface issues will be discussed in another symposium, scaled device potential inherent in Ge is more focused.

2. Discussion Points

We mainly discuss both (i) scaled gate stacks and (ii) source/drain issues.

(i) Gate stack issues specifically relevant to Ge.

(a) Ge oxidation does not follow the Deal-Grove kinetics. This fact should be taken into consideration for Ge gate stack formation process.

(b) EOT in Ge gate stacks is scalable down to 0.5 nm by using Ge-conscious high-k dielectric. HfO_2 is terrible on Ge, while M_2O_3 such as Y_2O_3 or Sc_2O_3 is rather friendly with Ge. This material selection is suggested by the standard Gibbs free energy consideration of oxides.

(c) The highest electron effective mobility in Ge n-FETs so far achieved is approximately 2,000 cm^2/Vsec on Ge (111), which is a half of the electron mobility in bulk Ge. This mobility exhibited the semiconductor like temperature dependence, which suggested the electron mobility was phonon-limited. Electron mobility higher than 1000 cm^2/Vs is viable in Ge MOSFETs with 0.8 nm EOT. It is surely scalable down to 0.5 nm EOT.

(d) Electron mobility under high electric fields is significantly improved on atomically flat Ge surfaces, which is prepared by pure H_2 annealing at high temperature.

(e) A lighter effective carrier mass is beneficial for the carrier mobility but too light one make the EOT scaling impossible owing to the quantum capacitance. It is luckily moderate in Ge. High carrier mobility is maintained in highly doped Ge thanks to less coulombic scattering probability because of higher dielectric constant of Ge.

(f) Gate stack reliability is now challenging, even though initial gate stack properties seem to be ok. Since Ge-O bonding is "weaker" than Si-O one, GeO_2/Ge interface can be better than SiO_2/Si thanks to "more flexible" bonding at the interface. It might be, however, worse in terms of the gate stack reliability owing to the weaker bond. Thus, GeO_2 will not be used for Ge gate stacks, and new dielectric film engineering must be considered. Y_2O_3-doped GeO_2 is proposed for Ge gate stack reliability solution.

(ii) Source/drain issues

(a) p/n junction leakage due to the narrower energy band gap in Ge is a big concern for low power applications. The source/drain leakage current in Ge FET is actually much higher than those in Si one in the literatures. If it cannot certainly be solved, conventional type of Ge FETs will not be practically usable. It is reported that the surface passivation layer is critical for reducing the junction leakage and achieving the tight distribution of junction leakage.

(b) The contact resistance is one of the most critical in terms of scaled CMOS performance. We have studied about metal/Ge Schottky characteristics and Fermi-level pinning, which is definitely against the low ohmic contact resistance. Two methods are introduced to alleviate the FLP on Ge.

3. Conclusion

Concerning the question whether Ge is substituting for Si, I am surely positive about Ge CMOS. However, I am also surely negative about 100% substitution of Si with Ge. More importantly, I would say Ge research is great fun.

(*) A. Toriumi and T. Nishimura, JJAP **57**, 010101 (2018).